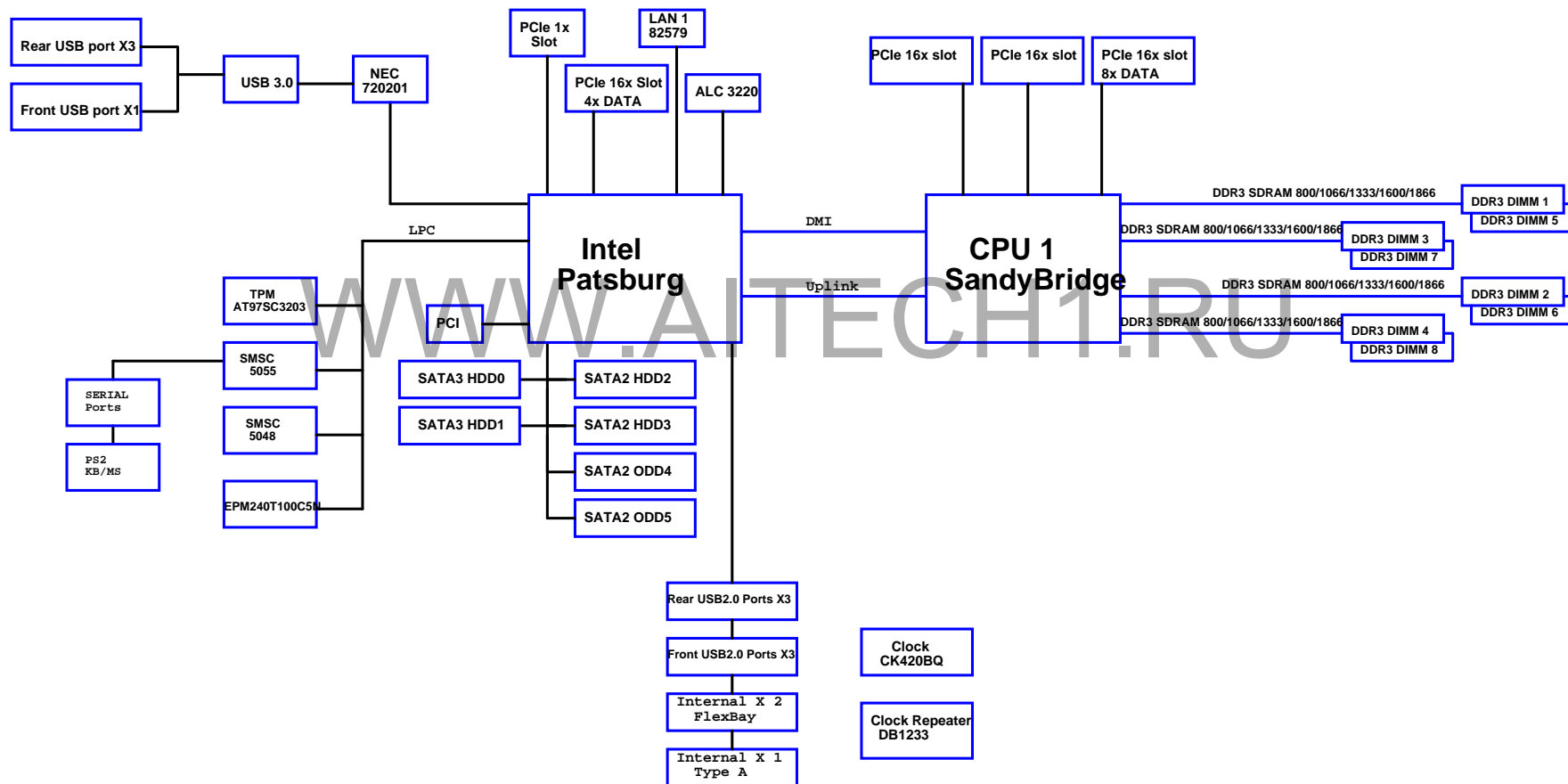
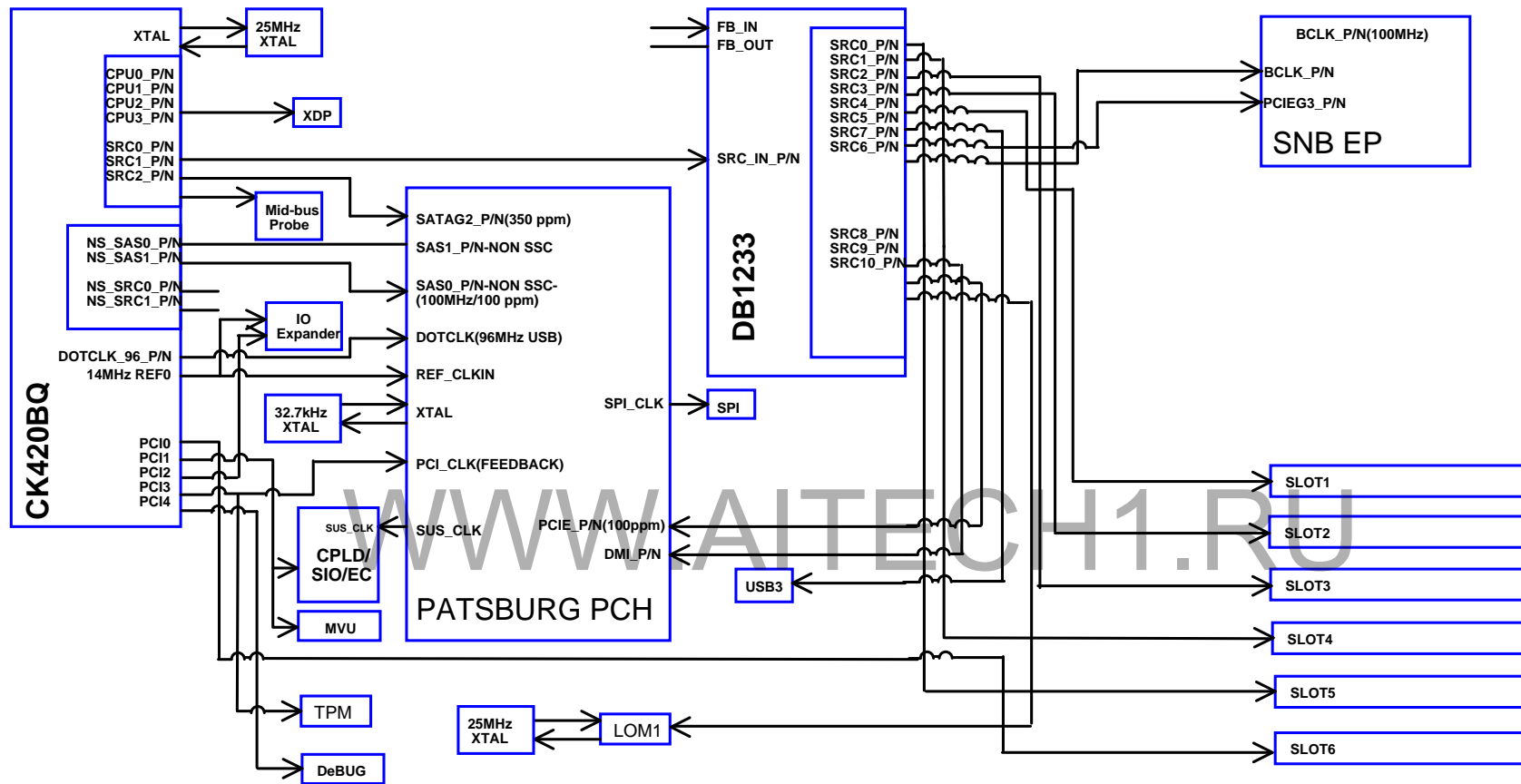
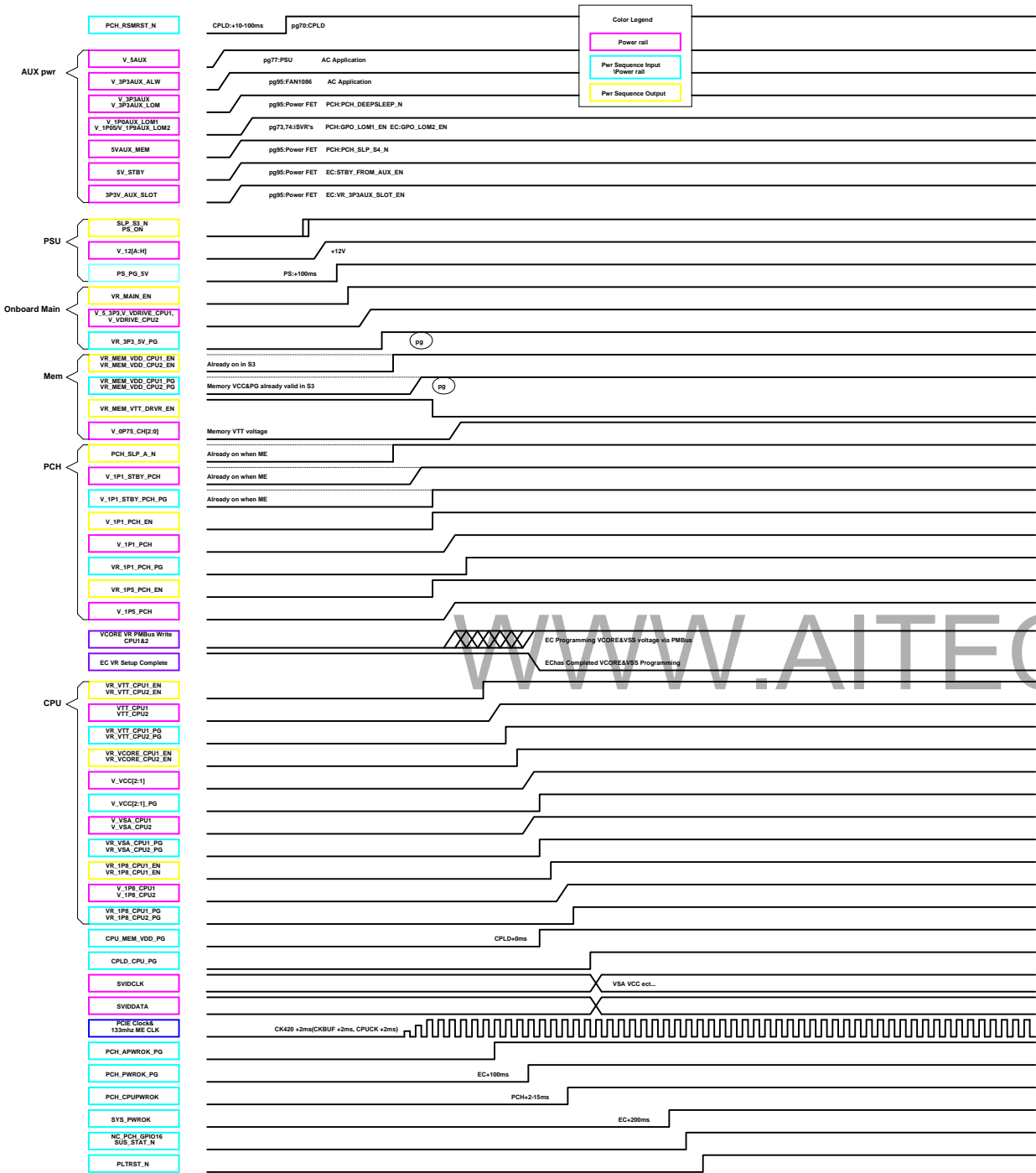


Bells 3





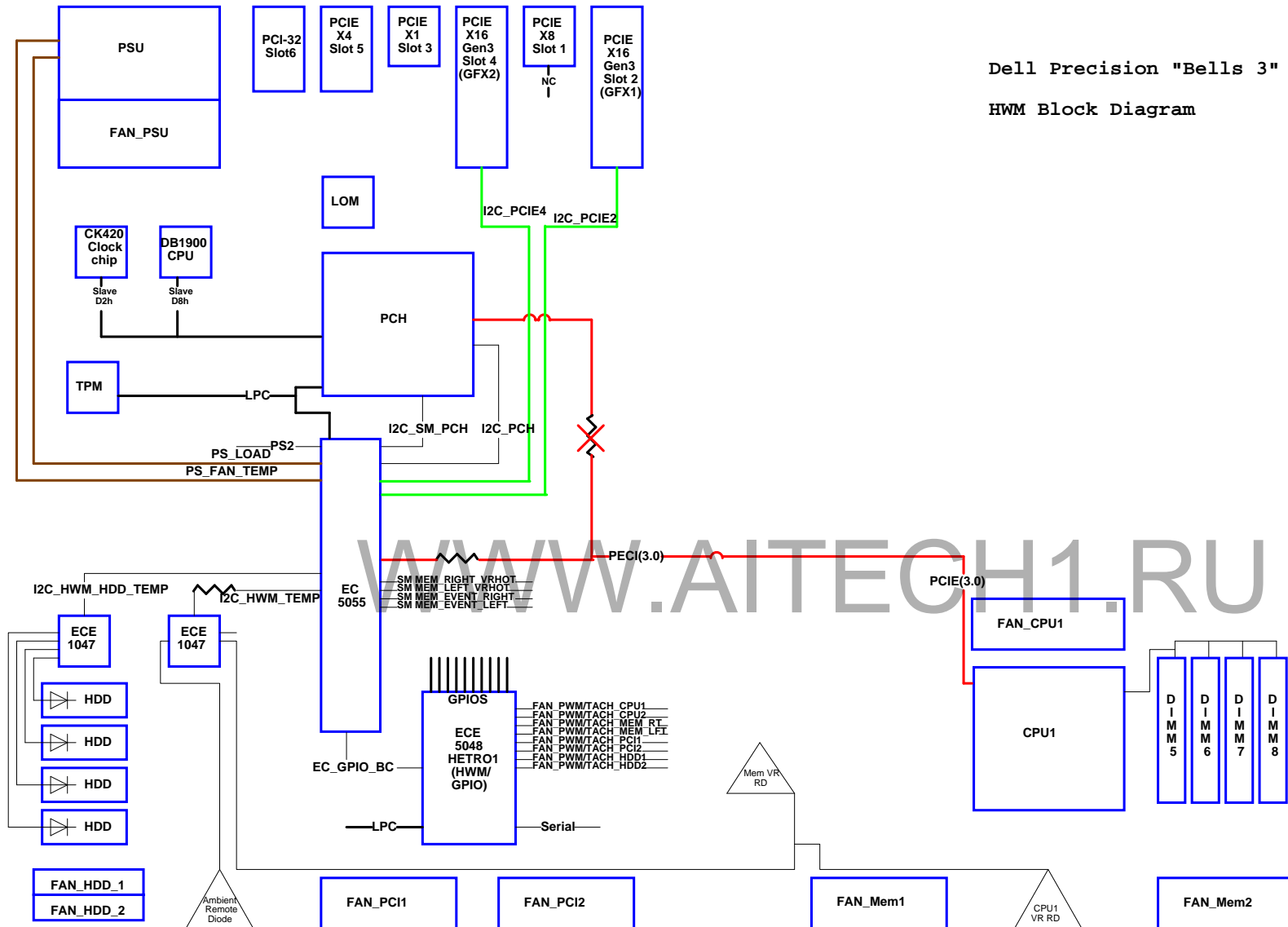
Bells 3
Clock Block Diagram

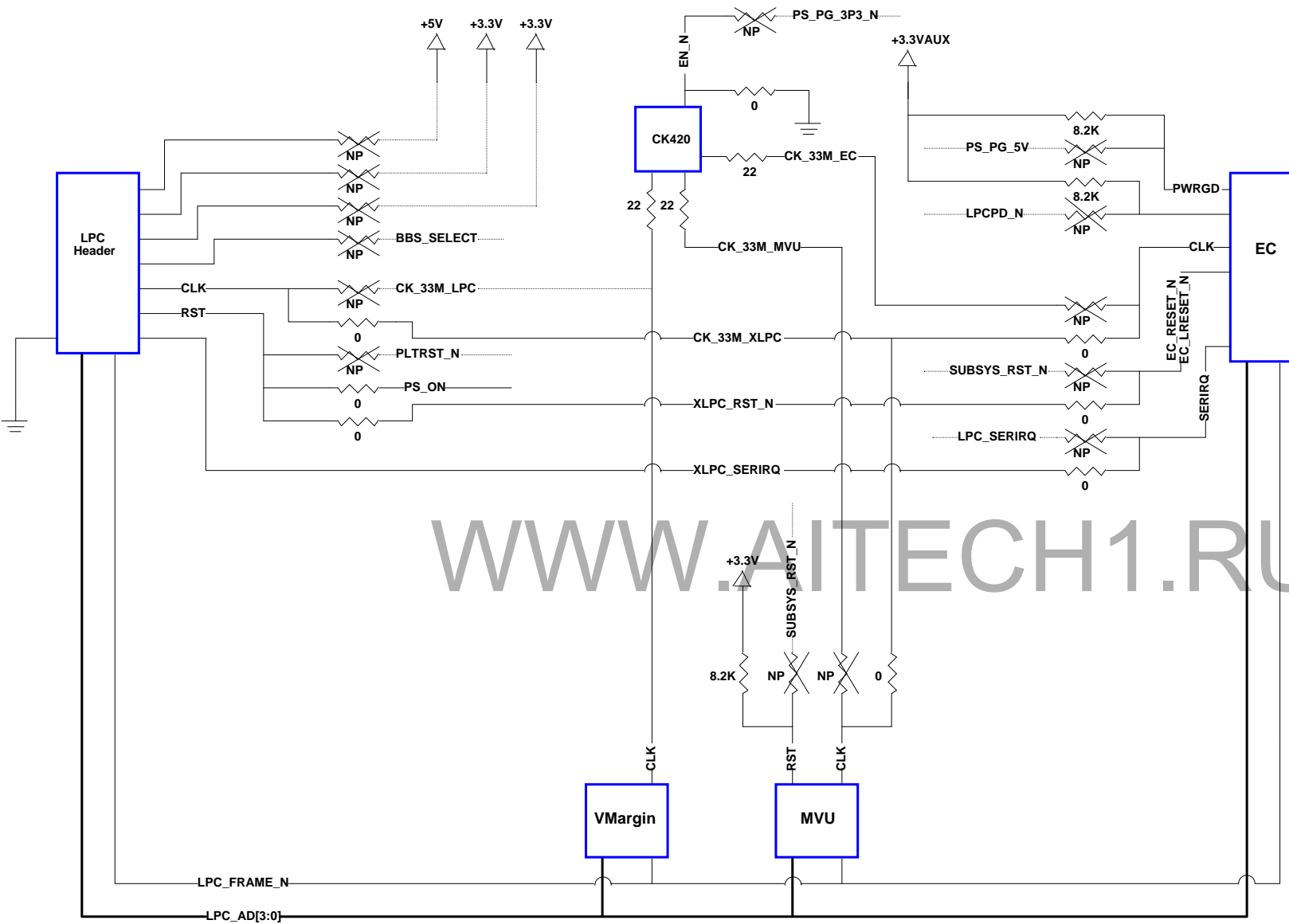


Bells 3 Power Sequence

Dell Precision "Bells 3"

HWM Block Diagram






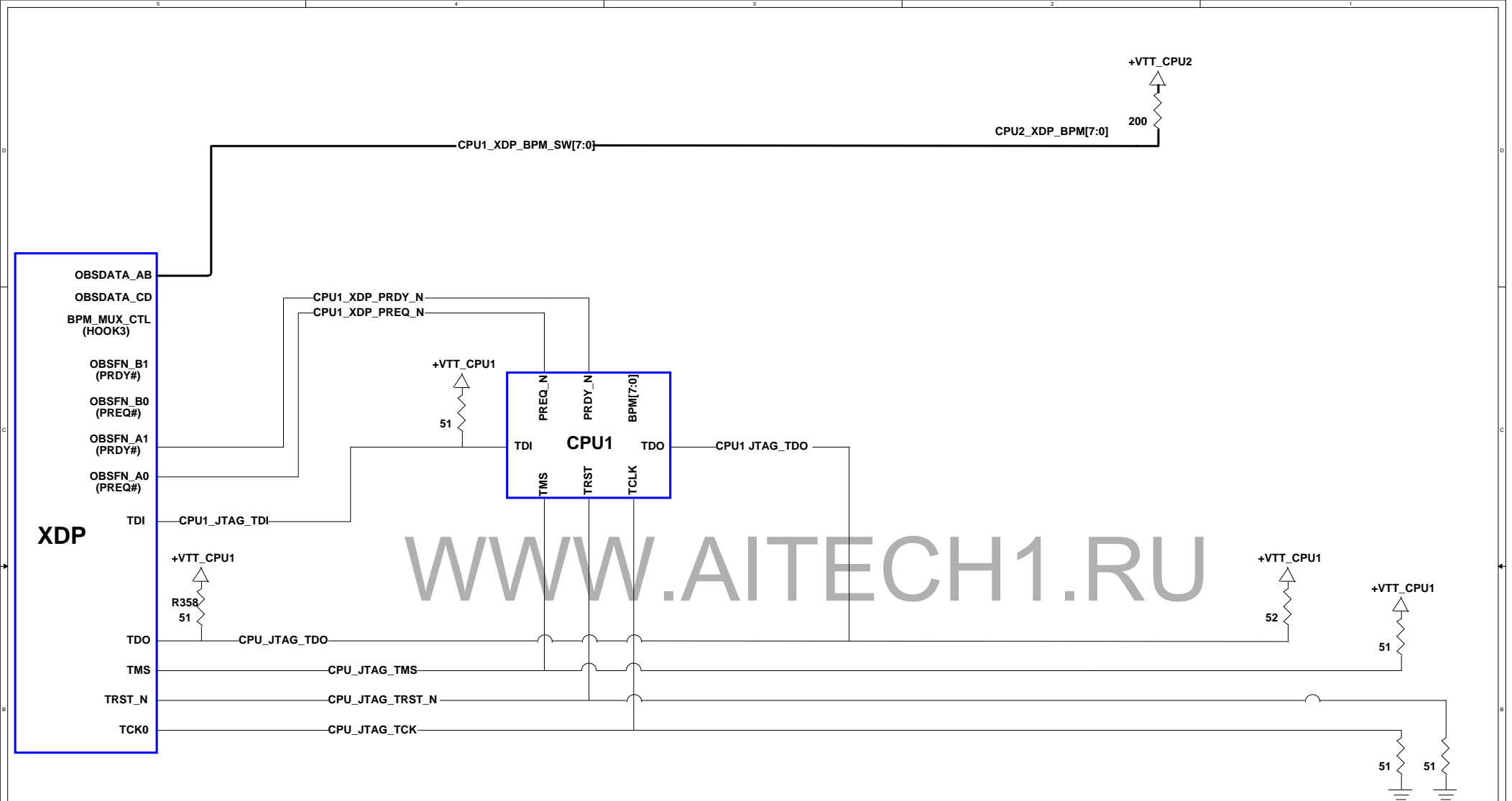
WWW.AITECH1.RU

For normal operation, the NP resistors would be re-populated and all other resistors (except for the 22ohm series terminations on the clock chip) would be de-popped.

**Bells3 XLPC
Control Diagram**

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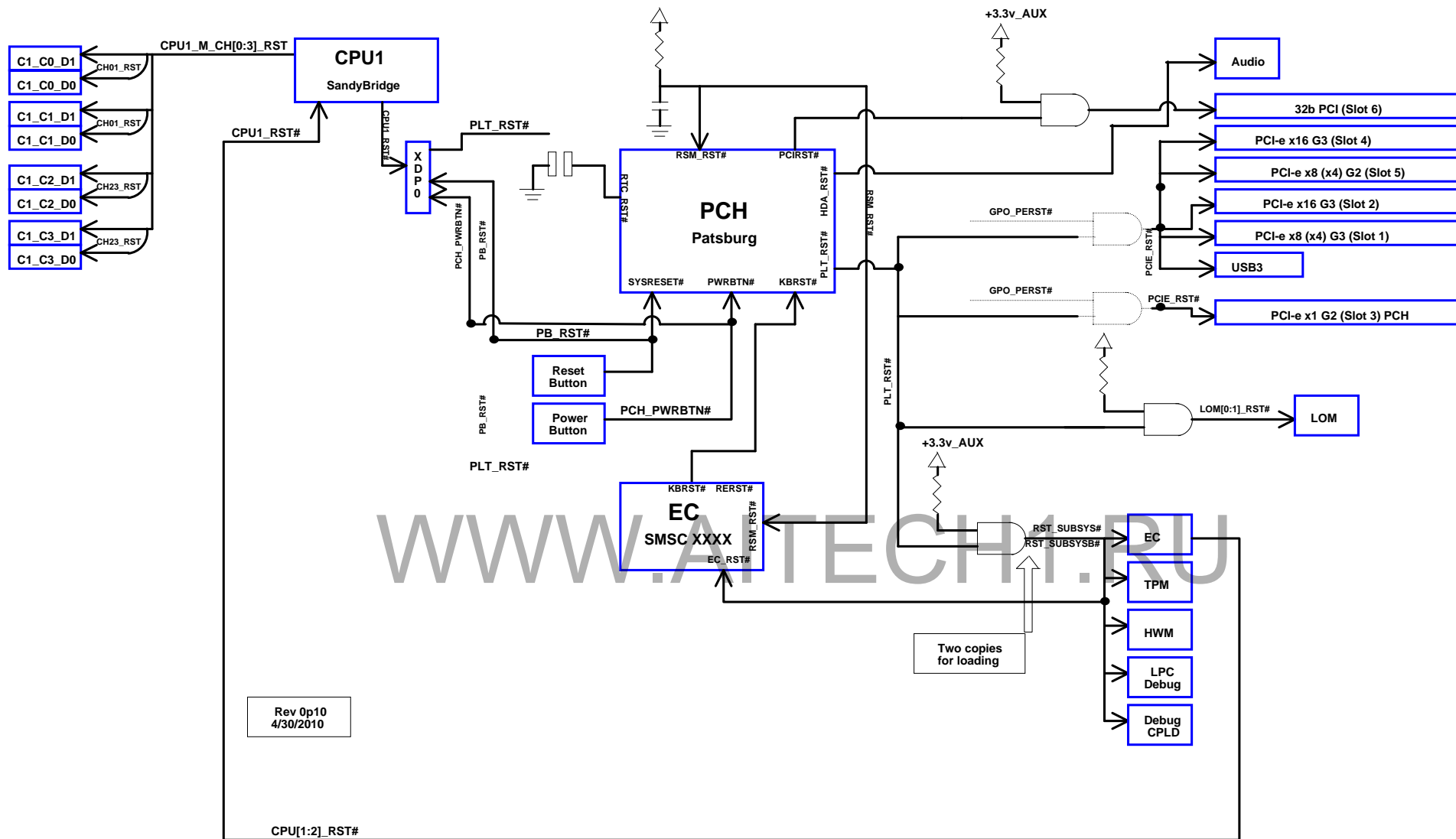
	
Title SCHEM,PMA,Bells 3	
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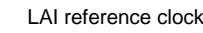
Debug Port Design Guide 0.95 Routing Guidelines:

- TCK/TMS max trace length = 1.5ns
- PREQ#/PRDY# max trace length = 1.5ns
- BPM max trace length between MUX and CPU = 10"
- BPM max trace length between MUXes = 8ns
- All BPM net lengths should match as a group to within +/-50ps
- All BPM nets must have 200ohm VTT terminations near CPU

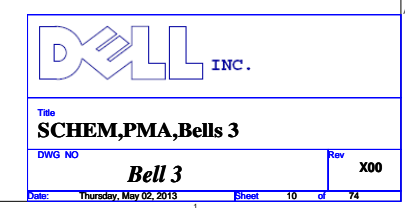
Bells 3 CPU XDP map



Bells3 Reset map



RoseCity-PG158-159



DDR_CH0

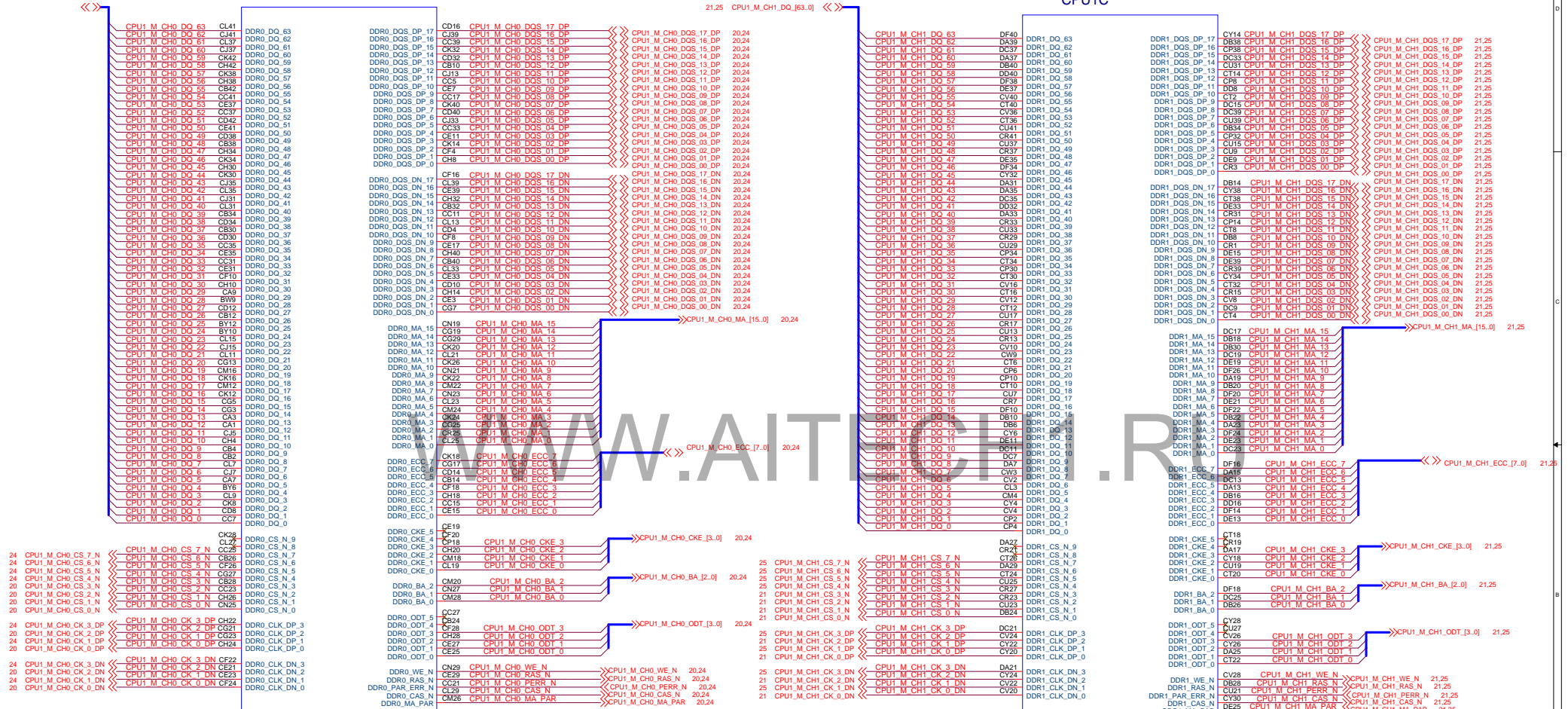
DDR_CH1

CPU1B

CPU1C

2024 CPU1_M_CH0_DQ_[63..0]


21,25 CPU1_M_CH1_DQ_[63..0] <<>



RoseCity-PG23

DSR-Pg22&23

RoseCity-PG22

	
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DDR_CH2

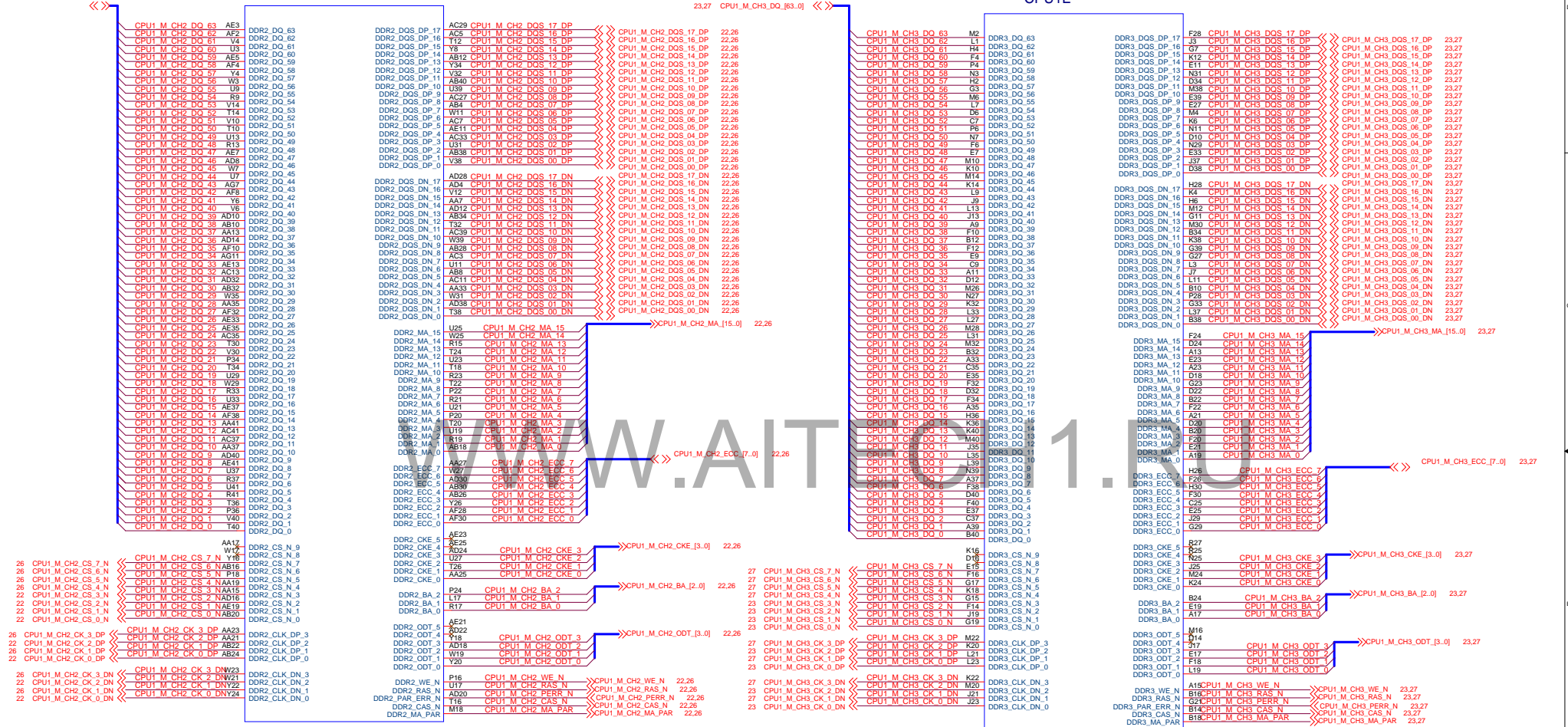
DDR_CH3

CPU1D

CPU1E

22.26 CPU1_M_CH2_DQ_[63..0]

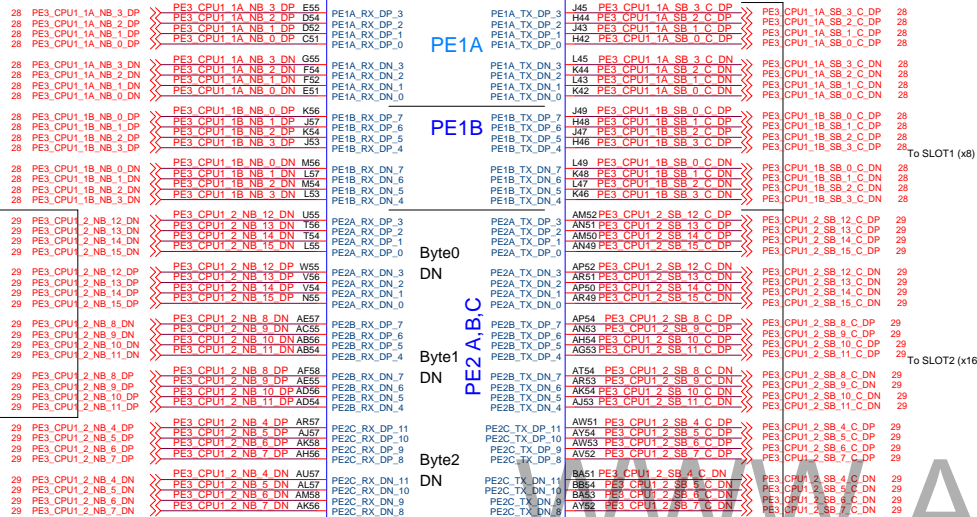
23.27 CPU1_M_CH3_DQ_[63..0]



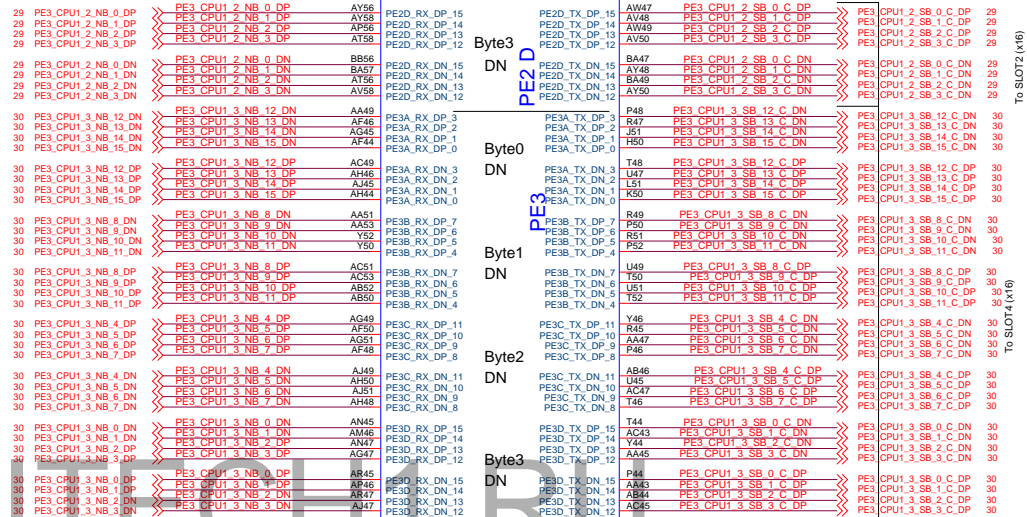
RoseCity-PG23

RoseCity-PG22

CPU1F



CPU1G



SandyBridge_EPEX_EDS_Vol1_26601.0.5.pvd Figure 1-3 pg.16

Port0	Port1	Port2	Port3
DMI	PE1[A:B]	PE2[A:B:C:D]	PE3[A:B:C:D]
IOU2---IOU2		IOU0	IOU1
DMI to PCH	X4 slot	X16 slot	X16 slot
	X4 to PCH		



Title
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DWG NO

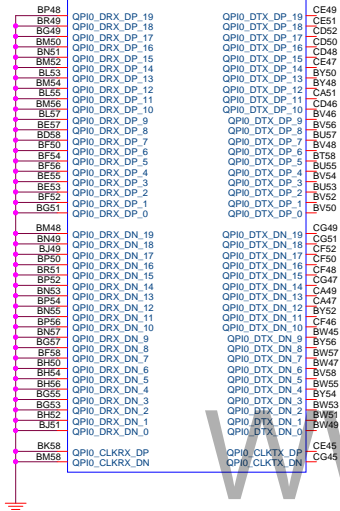
Bell 3

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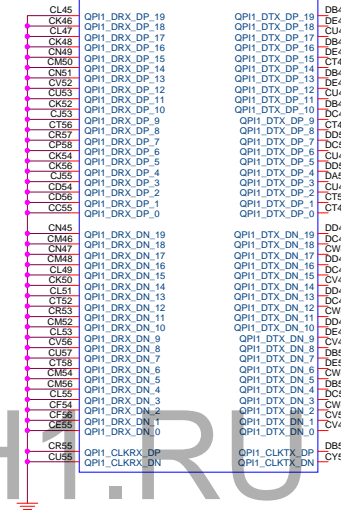
QPI0 interface

CPU1I

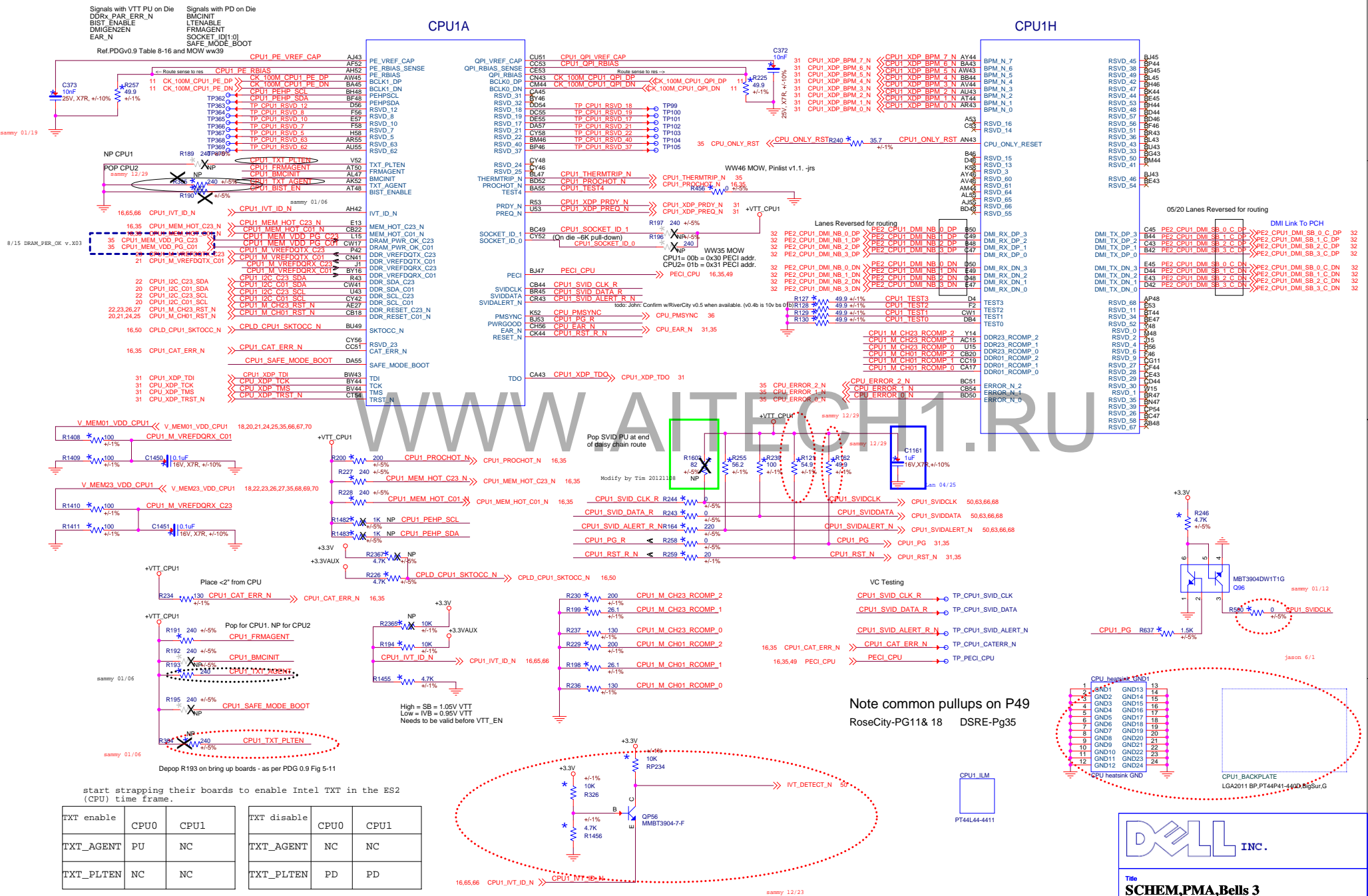


QPI1 interface

CPU1J



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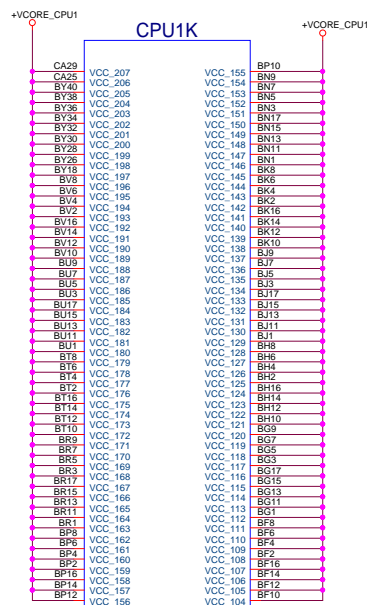


Title
SCHEM,PMA,Bells 3

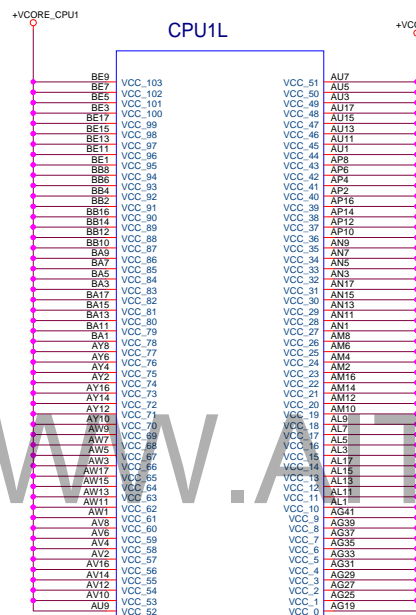
Bell 3

X00

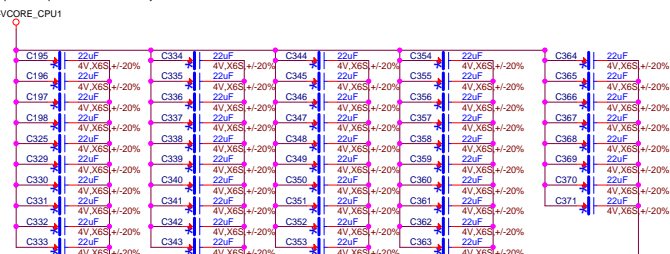
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RoseCity-PG31



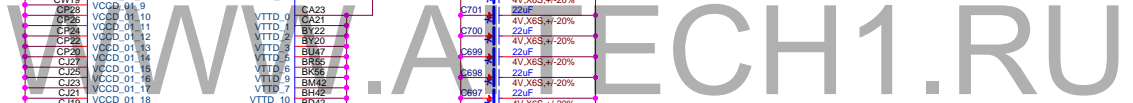
RoseCity-PG31




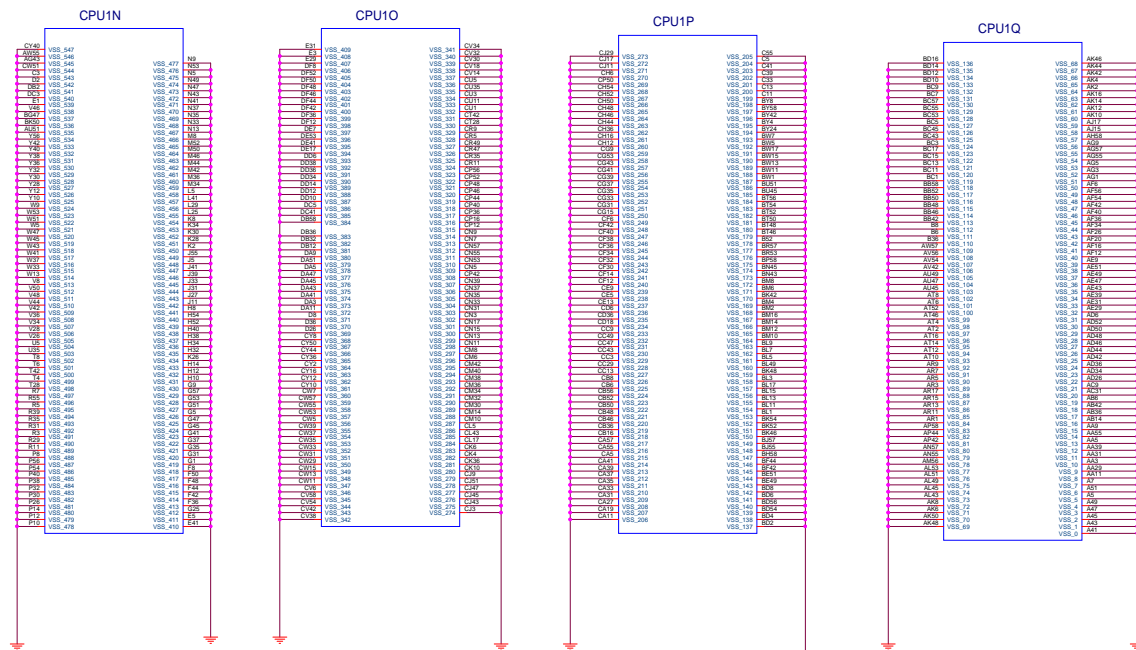
Title
SCHEM,PMA,Bells 3

Bell 3

Rev	X00
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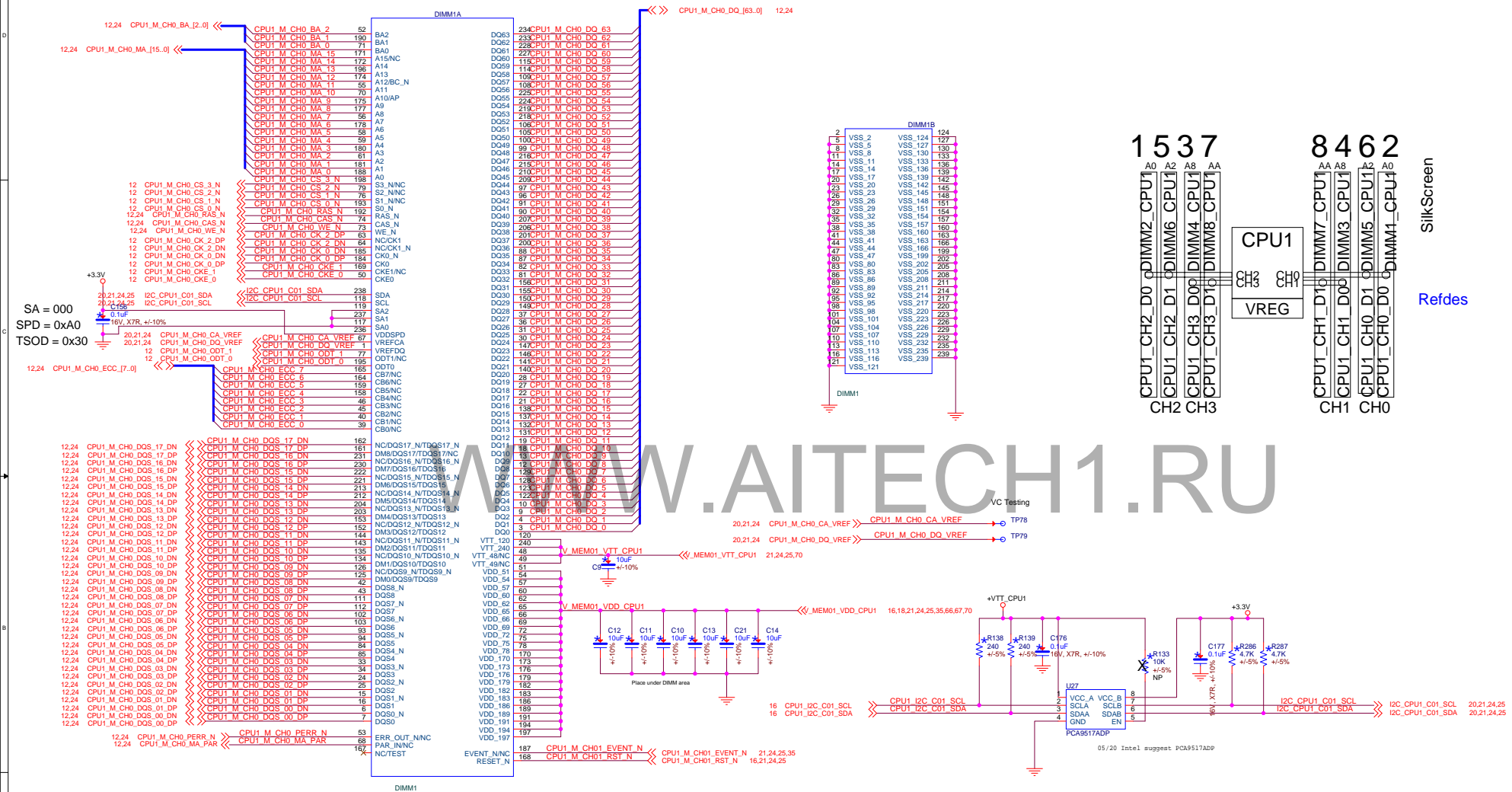


			
Title SCHEM, PMA, Bells 3			
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<i>Bell 3</i>			
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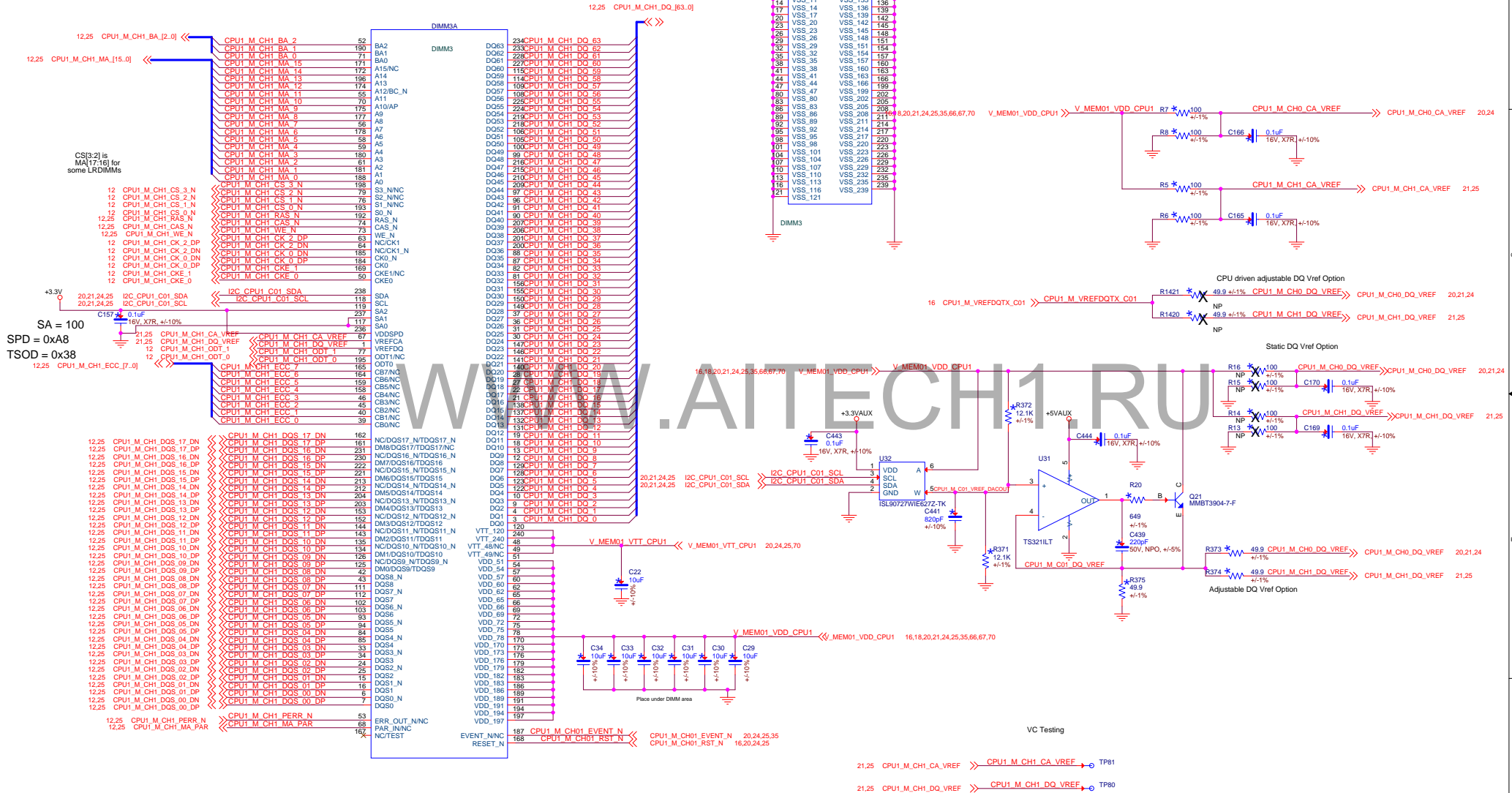


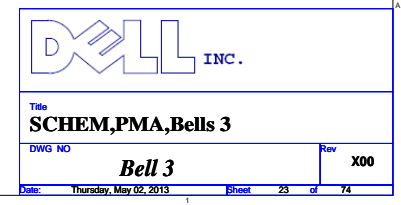
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CPU1_CH0_D0

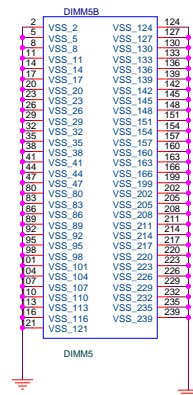
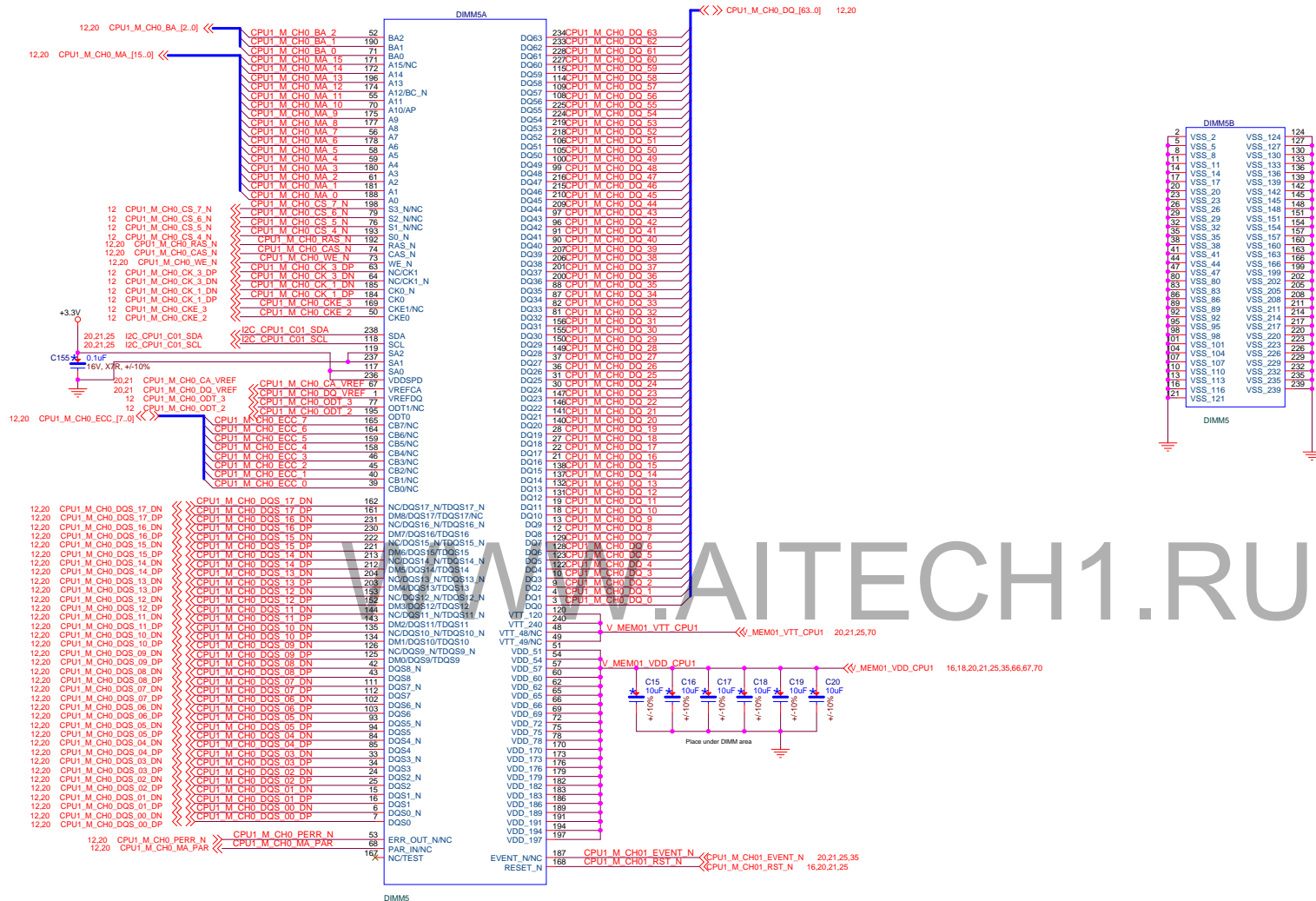


CPU1_CH1_D0

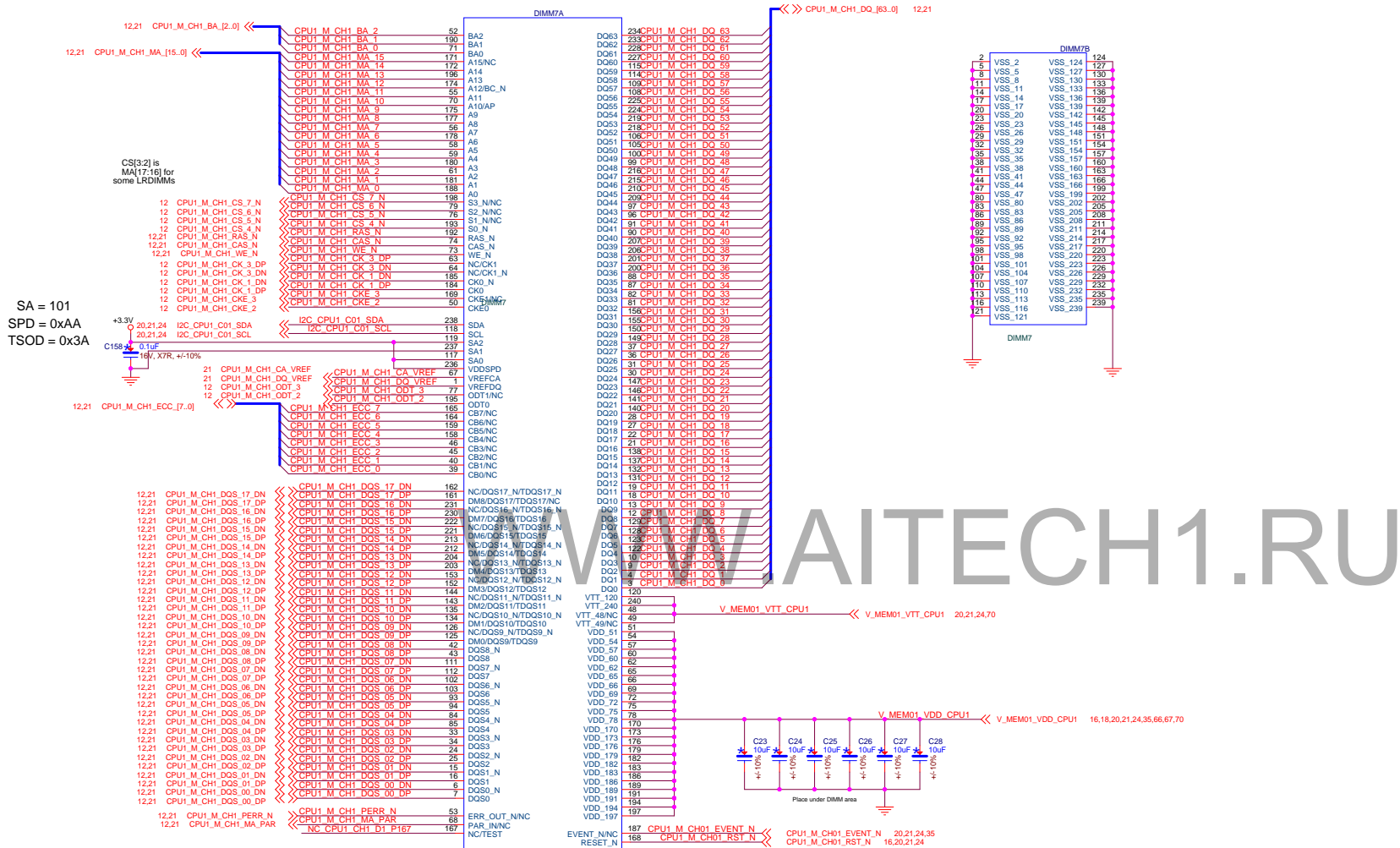


[illegible]

CPU1_CH0_D1



CPU1_CH1_D1



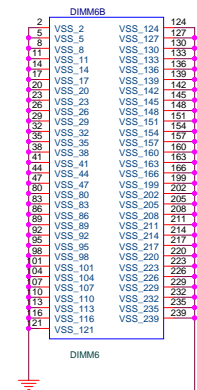
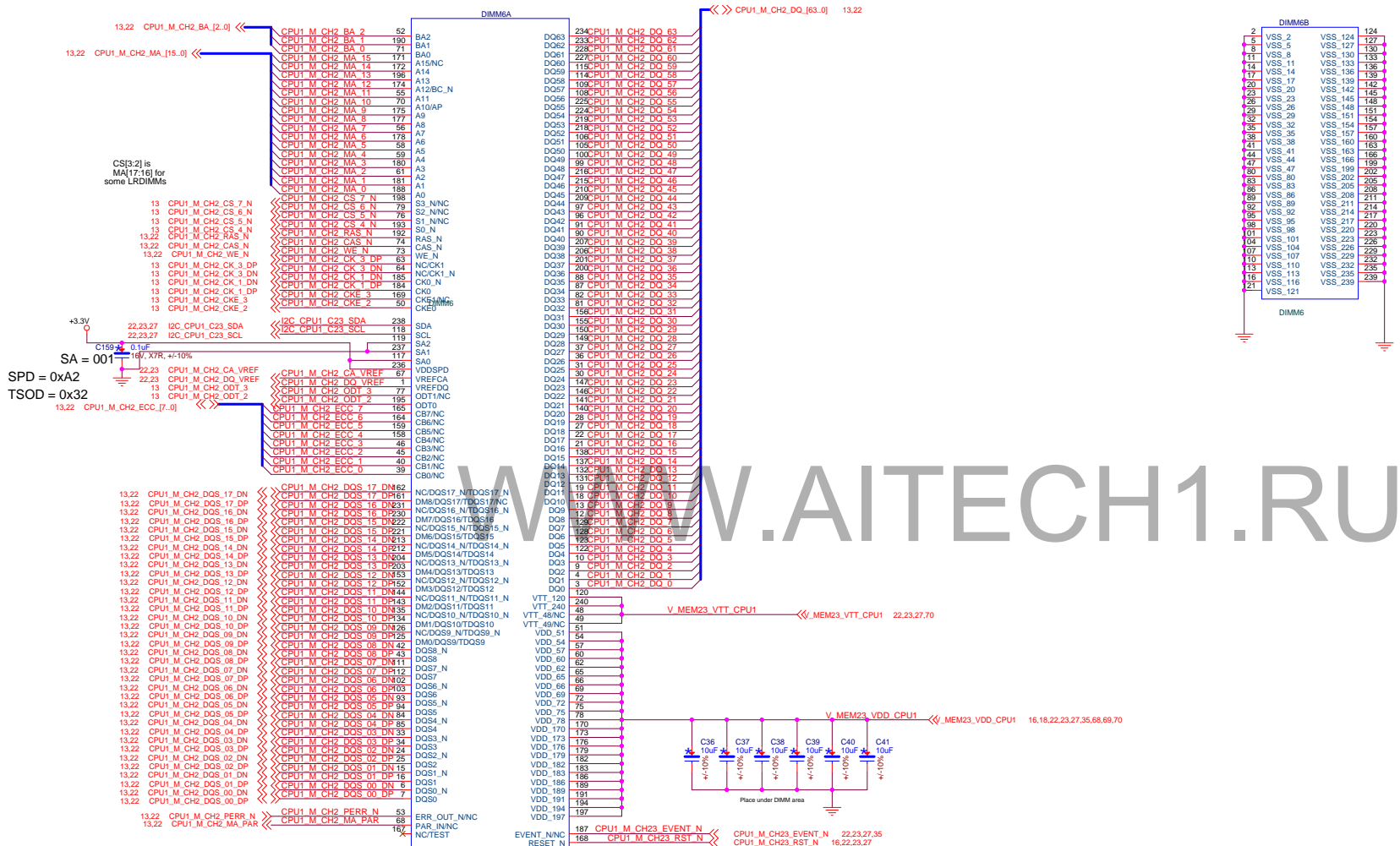
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SCHEM,PMA,Bells 3

DWG NO	
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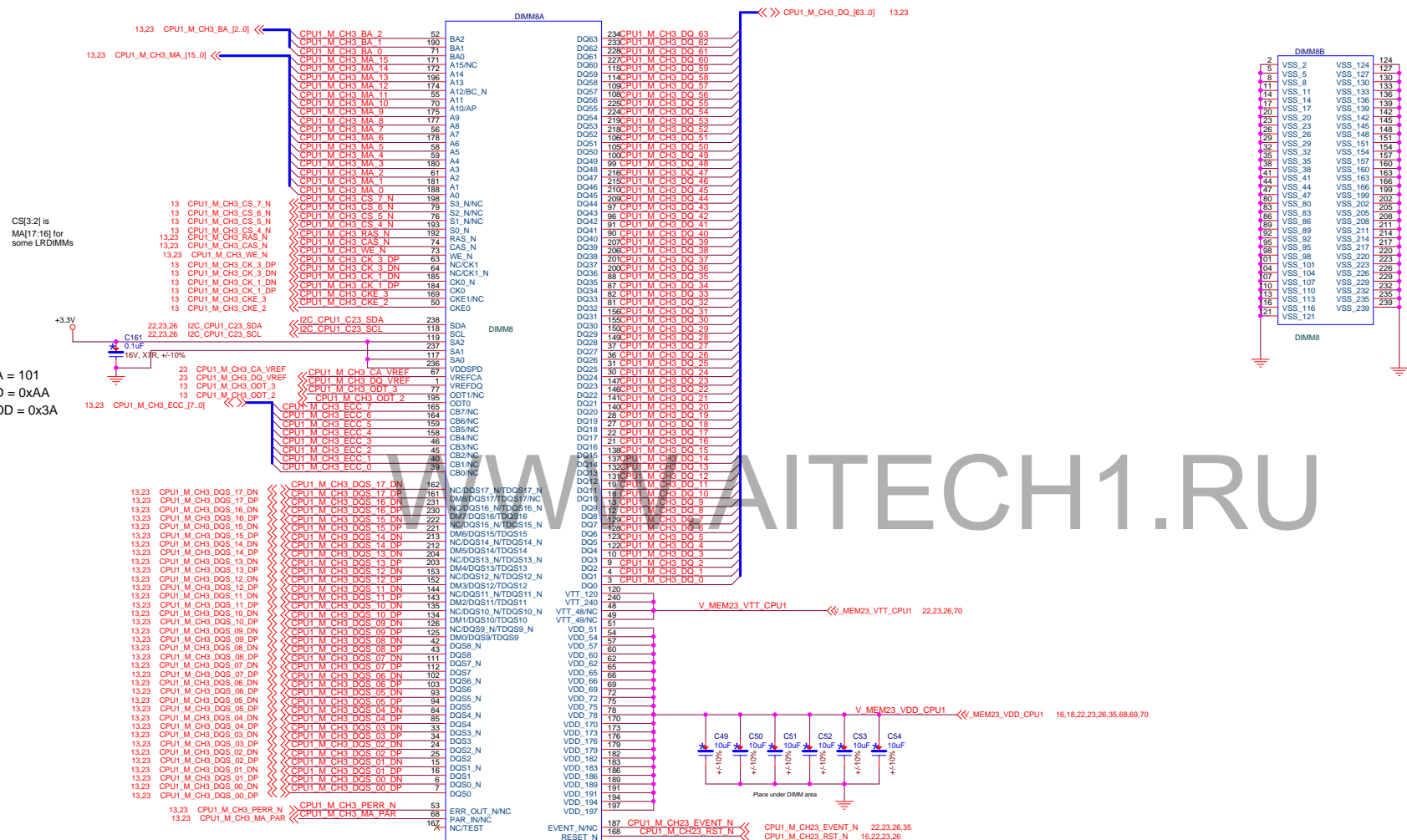
Bell 3

X00

CPU1_CH2_D1



CPU1_CH3_D1



Title
SCHEM,PMA,Bells 3

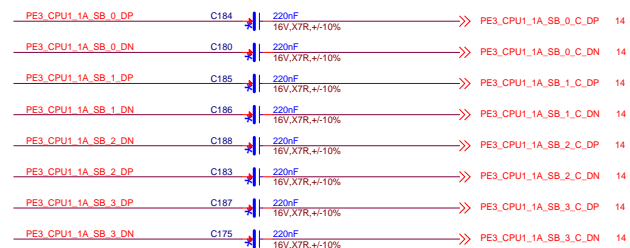
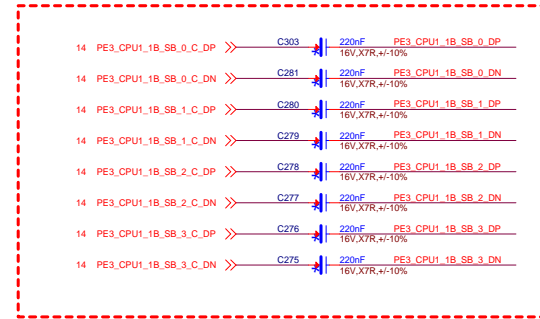
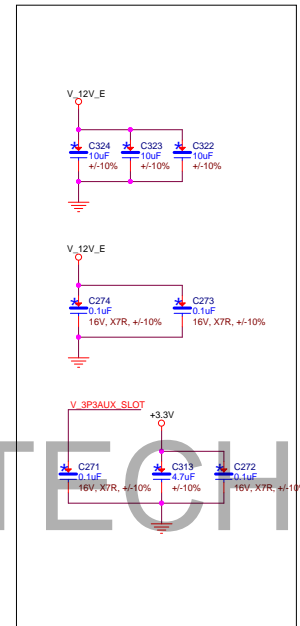
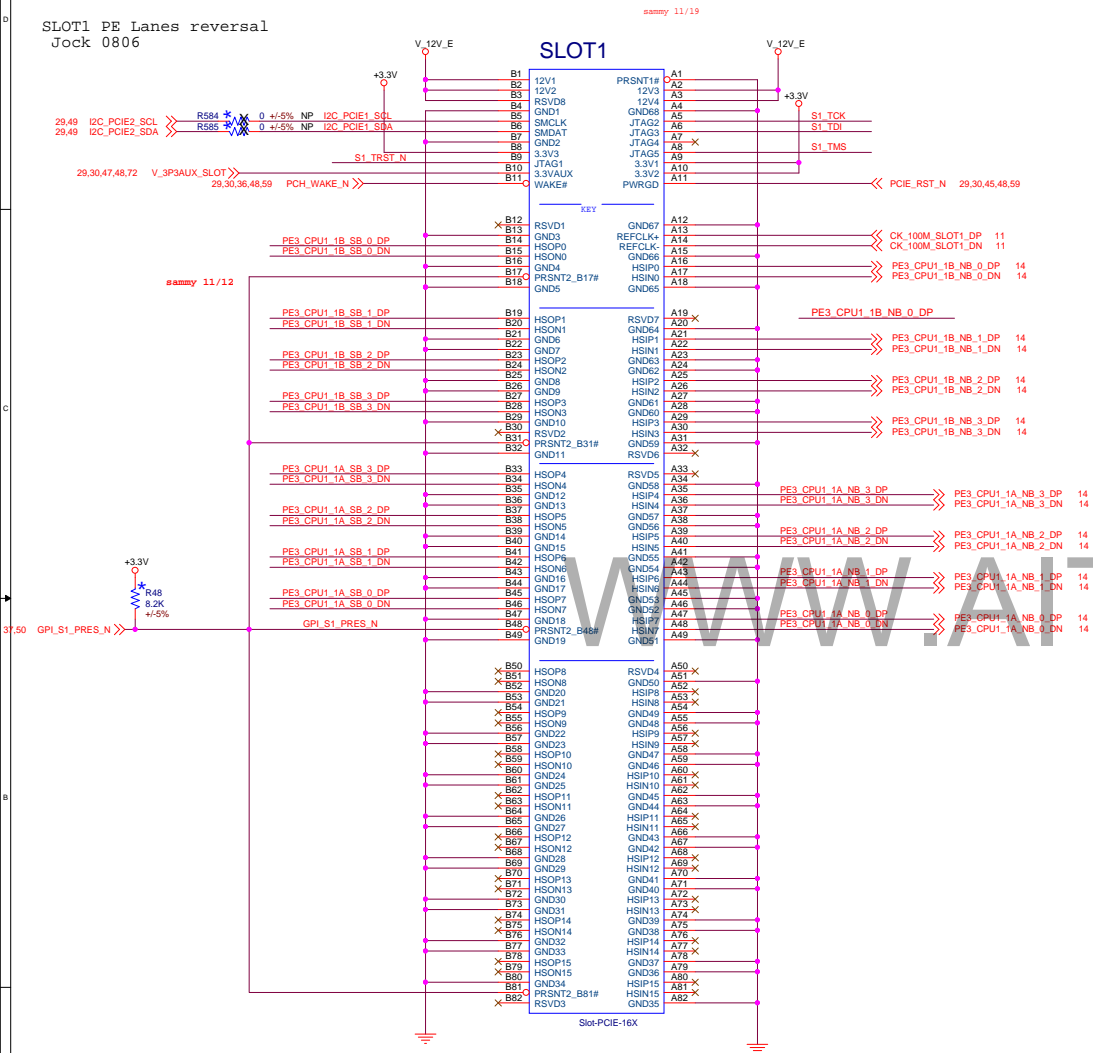
DWG NO	
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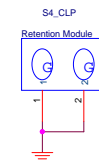
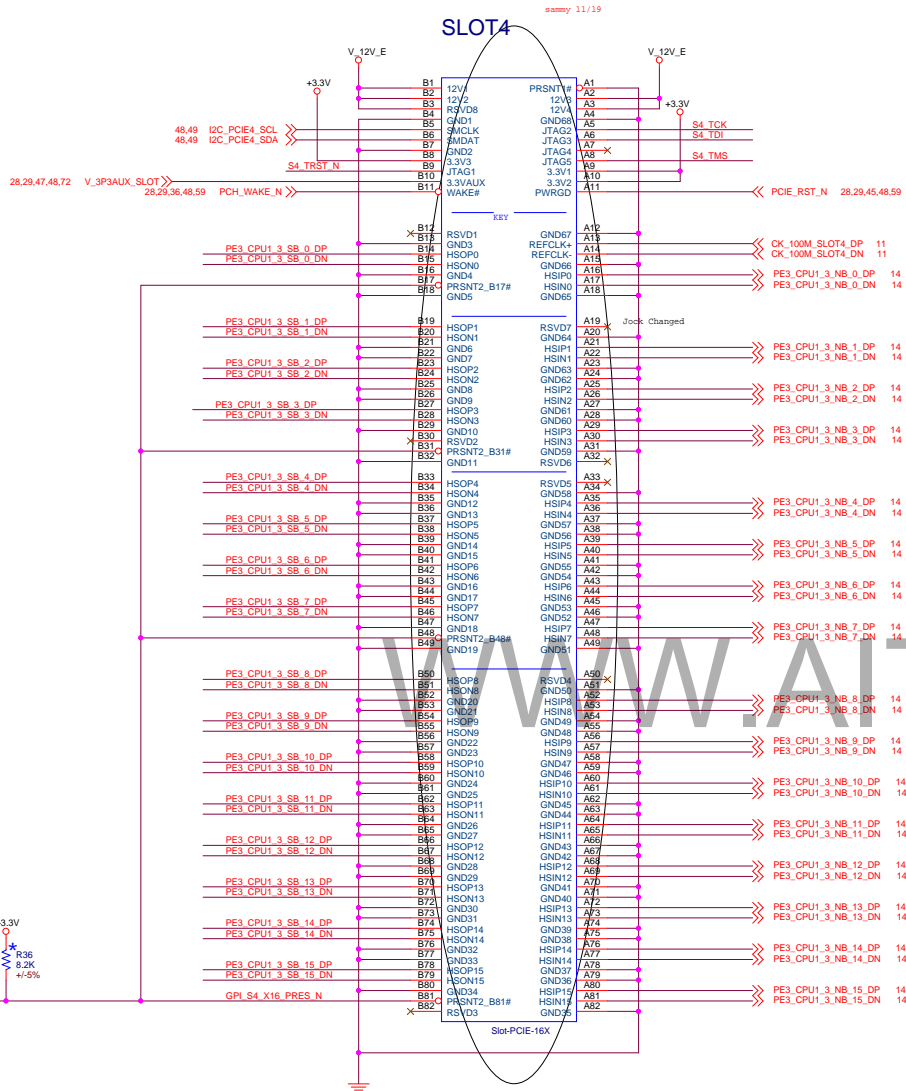
Bell 3

X00

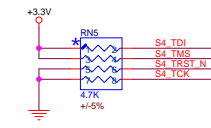
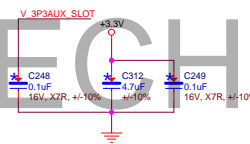
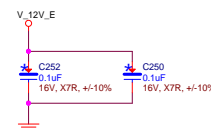
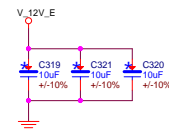
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SLOT1 PE Lanes reversal
Jock 0806





PCI-E x16 slot decoupling



NOTE: PCIe naming convention is:
EXP_[UpstreamDevice]_[Port]_[V]_[SB]_[LANE]_[C]_[DPIDN]

Placed by SLOT

14	PE3_CPU1_3_SB_0_C_DP	C253	220nF	PE3_CPU1_3_SB_0_DP
14	PE3_CPU1_3_SB_0_C_DN	C264	220nF	PE3_CPU1_3_SB_0_DN
14	PE3_CPU1_3_SB_1_C_DP	C263	220nF	PE3_CPU1_3_SB_1_DP
14	PE3_CPU1_3_SB_1_C_DN	C262	220nF	PE3_CPU1_3_SB_1_DN
14	PE3_CPU1_3_SB_2_C_DP	C261	220nF	PE3_CPU1_3_SB_2_DP
14	PE3_CPU1_3_SB_2_C_DN	C259	220nF	PE3_CPU1_3_SB_2_DN
14	PE3_CPU1_3_SB_3_C_DP	C258	220nF	PE3_CPU1_3_SB_3_DP
14	PE3_CPU1_3_SB_3_C_DN	C257	220nF	PE3_CPU1_3_SB_3_DN
14	PE3_CPU1_3_SB_4_C_DP	C256	220nF	PE3_CPU1_3_SB_4_DP
14	PE3_CPU1_3_SB_4_C_DN	C255	220nF	PE3_CPU1_3_SB_4_DN
14	PE3_CPU1_3_SB_5_C_DP	C254	220nF	PE3_CPU1_3_SB_5_DP
14	PE3_CPU1_3_SB_5_C_DN	C251	220nF	PE3_CPU1_3_SB_5_DN
14	PE3_CPU1_3_SB_6_C_DP	C247	220nF	PE3_CPU1_3_SB_6_DP
14	PE3_CPU1_3_SB_6_C_DN	C246	220nF	PE3_CPU1_3_SB_6_DN
14	PE3_CPU1_3_SB_7_C_DP	C245	220nF	PE3_CPU1_3_SB_7_DP
14	PE3_CPU1_3_SB_7_C_DN	C244	220nF	PE3_CPU1_3_SB_7_DN
14	PE3_CPU1_3_SB_8_C_DP	C243	220nF	PE3_CPU1_3_SB_8_DP
14	PE3_CPU1_3_SB_8_C_DN	C242	220nF	PE3_CPU1_3_SB_8_DN
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14	PE3_CPU1_3_SB_9_C_DN	C240	220nF	PE3_CPU1_3_SB_9_DN
14	PE3_CPU1_3_SB_10_C_DP	C239	220nF	PE3_CPU1_3_SB_10_DP
14	PE3_CPU1_3_SB_10_C_DN	C238	220nF	PE3_CPU1_3_SB_10_DN
14	PE3_CPU1_3_SB_11_C_DP	C237	220nF	PE3_CPU1_3_SB_11_DP
14	PE3_CPU1_3_SB_11_C_DN	C236	220nF	PE3_CPU1_3_SB_11_DN
14	PE3_CPU1_3_SB_12_C_DP	C235	220nF	PE3_CPU1_3_SB_12_DP
14	PE3_CPU1_3_SB_12_C_DN	C270	220nF	PE3_CPU1_3_SB_12_DN
14	PE3_CPU1_3_SB_13_C_DP	C269	220nF	PE3_CPU1_3_SB_13_DP
14	PE3_CPU1_3_SB_13_C_DN	C268	220nF	PE3_CPU1_3_SB_13_DN
14	PE3_CPU1_3_SB_14_C_DP	C267	220nF	PE3_CPU1_3_SB_14_DP
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14	PE3_CPU1_3_SB_15_C_DP	C265	220nF	PE3_CPU1_3_SB_15_DP
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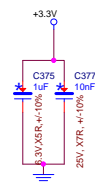
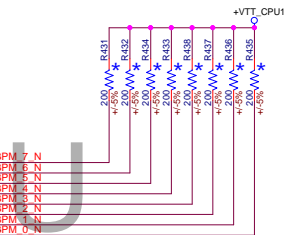
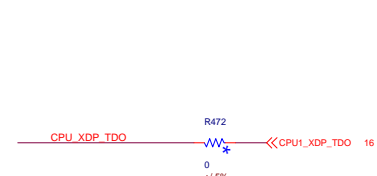
Title
SCHEM,PMA,Bells 3


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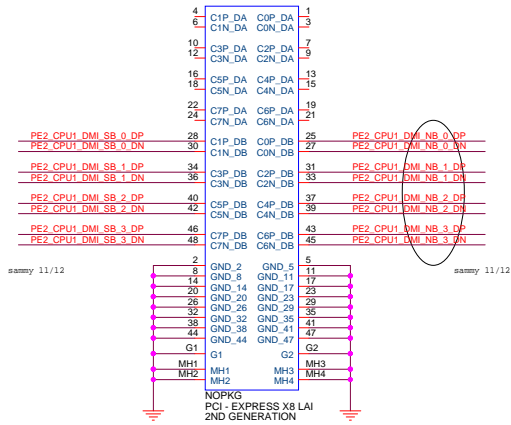
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LAI_DMI_PCIE



On SandyBridge side caps. Verify w/SI & layout

PCIe x4 Uplink port on CPU1/PCH

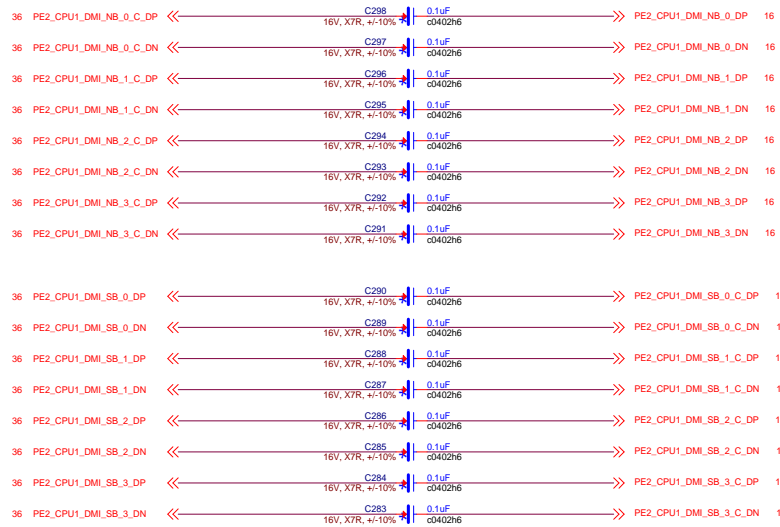
See Romley_PDG_Vol2_27178.0.5.pvd Table 14-28

Polarity (DP/DN) may be swapped.

Entire link assignment may be reversed:


SB_0 --> SB_3
SB_1 --> SB_2
SB_2 --> SB_1
SB_3 --> SB_0

To DMI on PCH




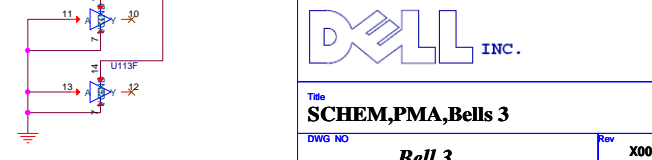
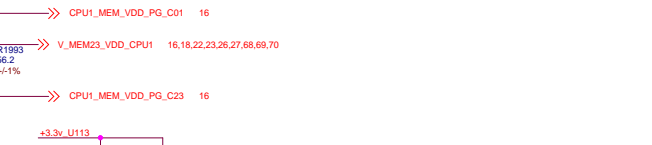
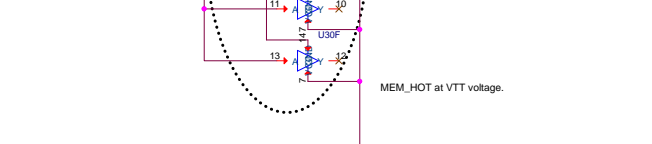
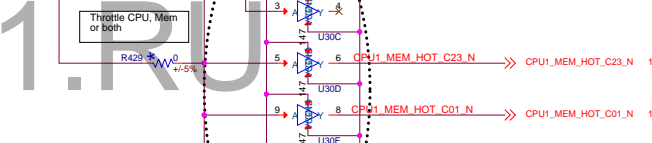
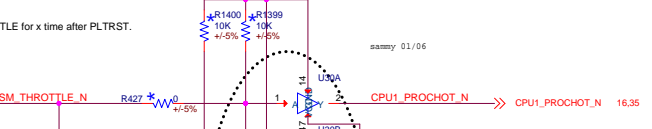
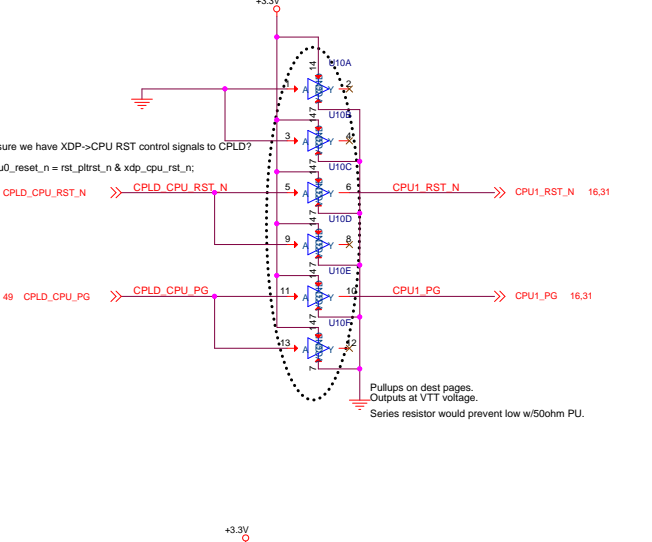
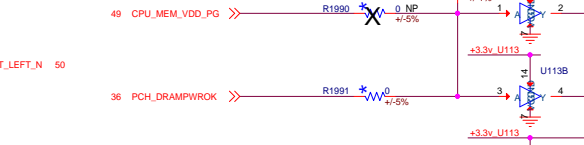
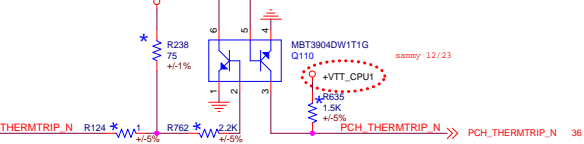
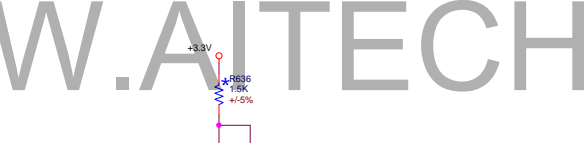
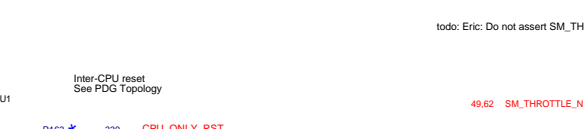
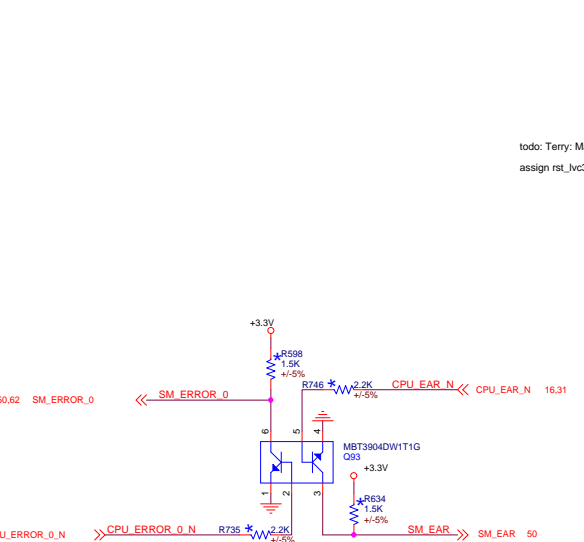
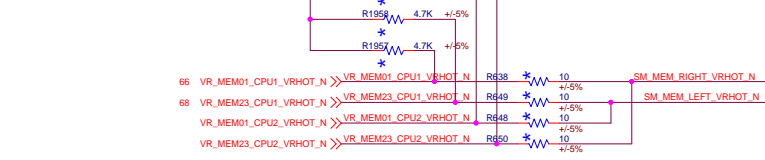
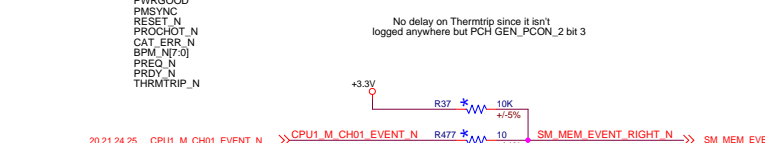
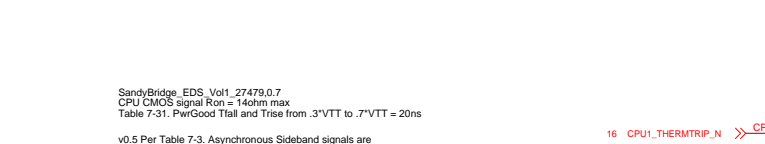
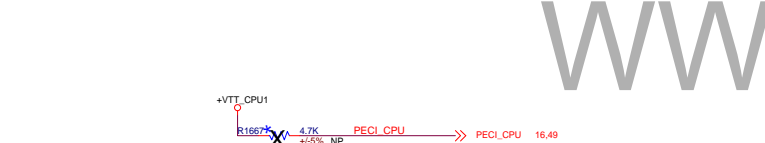
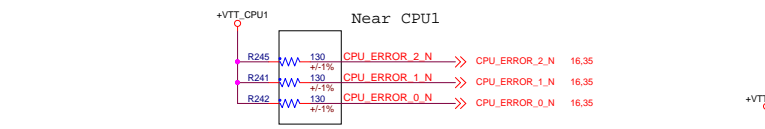
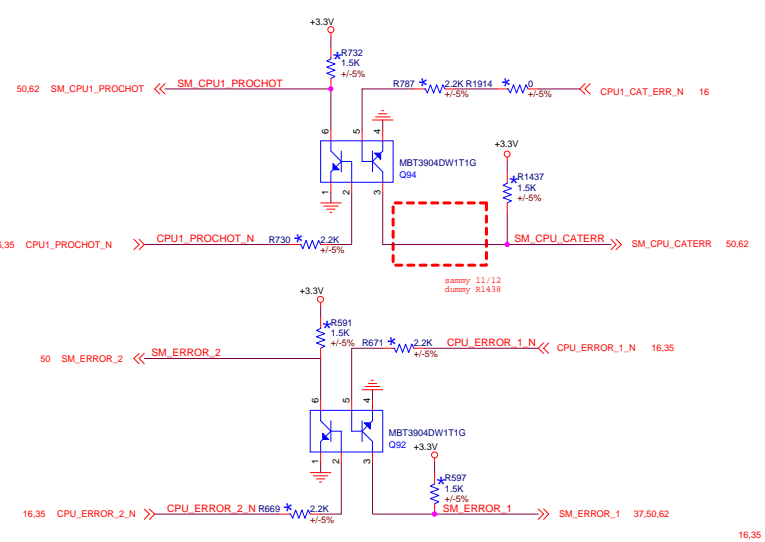
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todo: Terry: Make sure we have XDP->CPU RST control signals to CPLD?
assign rst_lv3_cpu0_reset_n = rst_pltrst_n & xdp_cpu_rst_n;

todo: Eric: Do not assert SM_THROTTLE for x time after PLTRST.

No delay on Therrtrip since it isn't
logged anywhere but PCH_GEN_PCON_2 bit 3

SandyBridge_EDS_Vol1_27479.0.7
CPU CMOS signal Ron = 140hm max
Table 7-31. PwrGood Tlalt and Trise from .3V VTT to .7V VTT = 20ns
PWRGOOD
PMSYNC
RESET_N
PROCHOT_N
CAT_ERR_N
BPM_N[7:0]
PRDY_N
PRDY_N
THRMTRIP_N



INC.

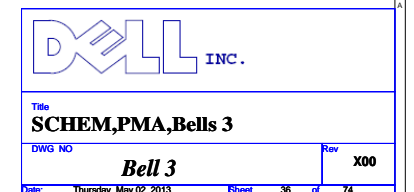
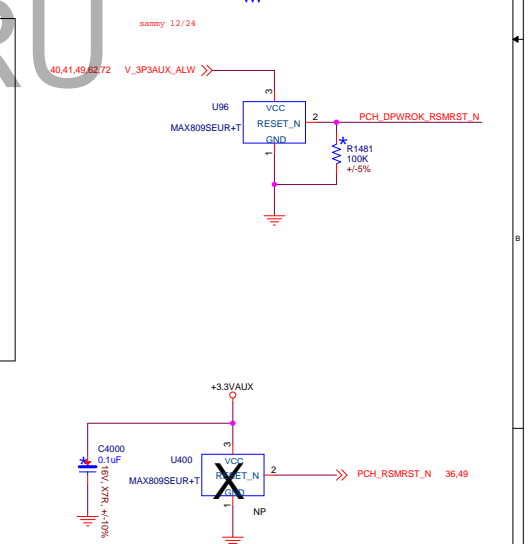
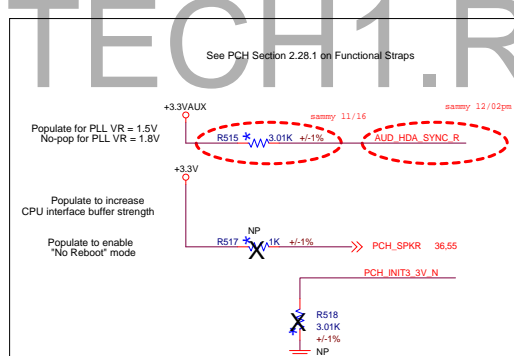
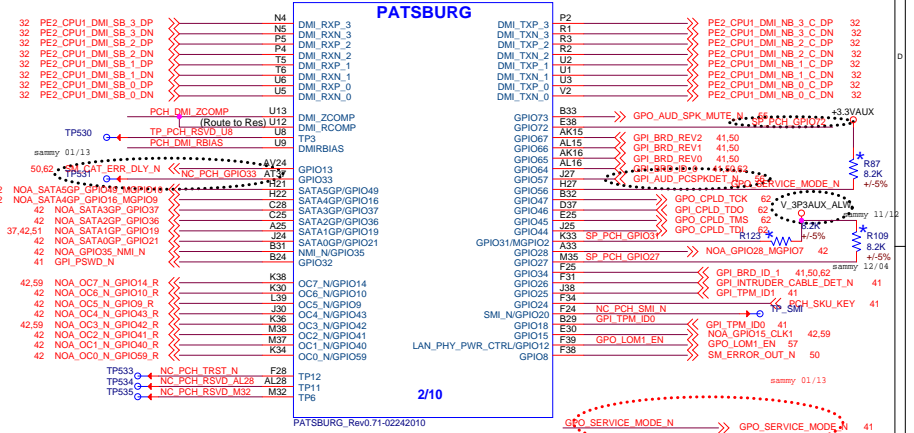
Title
SCHEM,PMA,Bells 3

DWG NO
Bell 3

Rev
X00

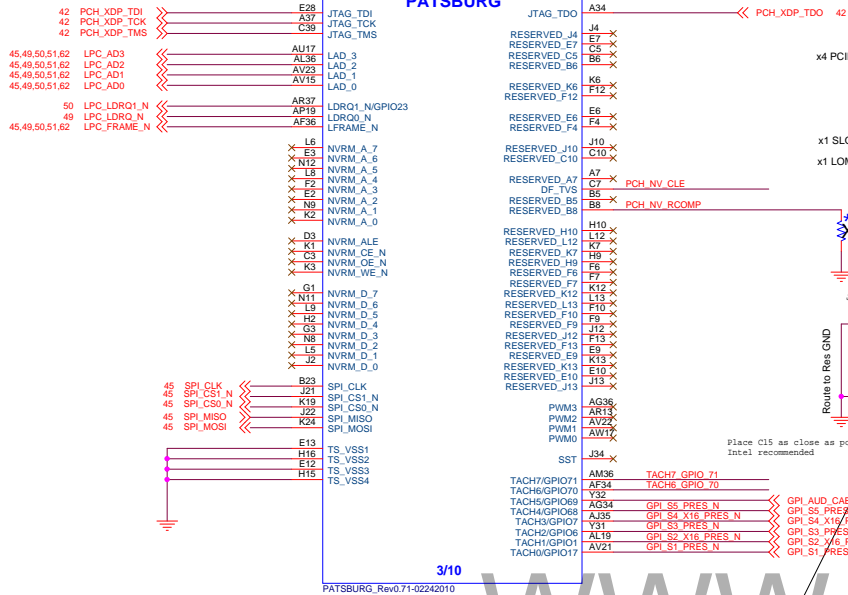
Date: Thursday, May 02, 2013 Sheet 35 of 74

U_PCH

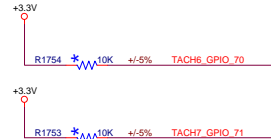


U_PCH

PATSBURG

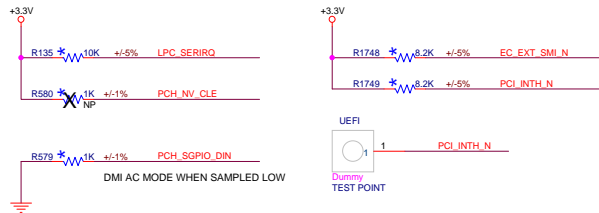
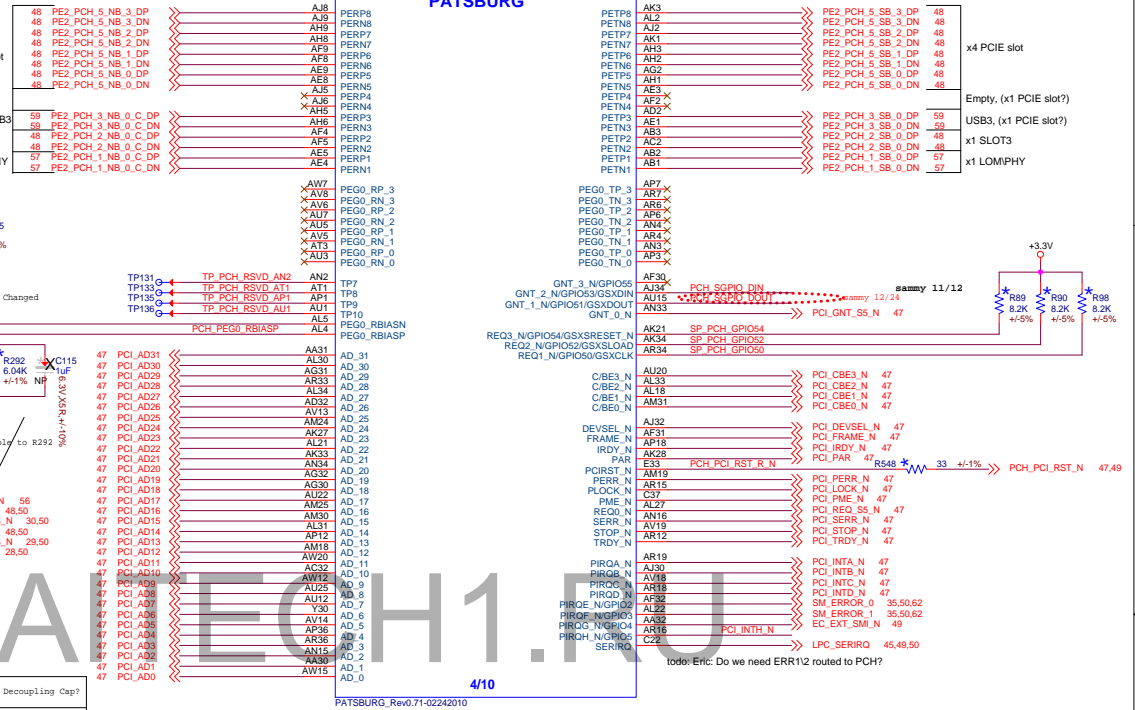


Via spacing (center to center)	Trace spacing (edge to edge)	Trace coupling length	Decoupling Cap?
>=50mil (or, no via)	>=5h (stripline) >=7h (microstrip)	<=0.3"	No Cap



U_PCH

PATSBURG



BOOT BIOS STRAPS		
DEFAULT 1,1: Weak PCH Internal PU		
PCH_SGPIO_DOUT	SATA1GP_GPIO19	
0	0	LPC
0	0	NAND
1	0	PCI
1	1	SPI

51

NOA_SATA1GP_GPIO19 36,42,51

DELL INC.

Title
SCHEM,PMA,Bells 3

DWG NO
Bell 3

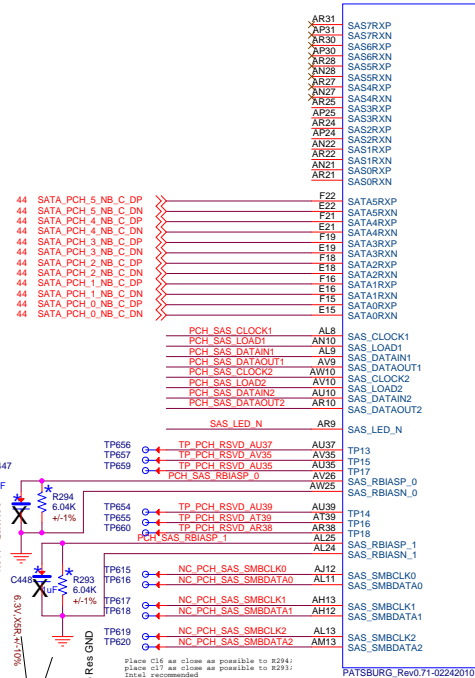
Rev
X00

Date
Thursday, May 02, 2013

Sheet
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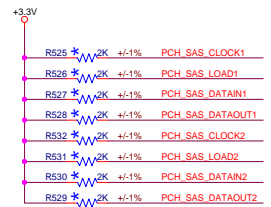
U_PCH

PATSBURG



Via spacing (center to center)	Trace spacing (edge to edge)	Trace coupling length	Decoupling Cap?
>=26mil	>=3h (stripline) >=3h (microstrip)	<=0.3"	duf/decap Required

SGPIO Pull Ups pg. 88
Place PU within 2" from PBG

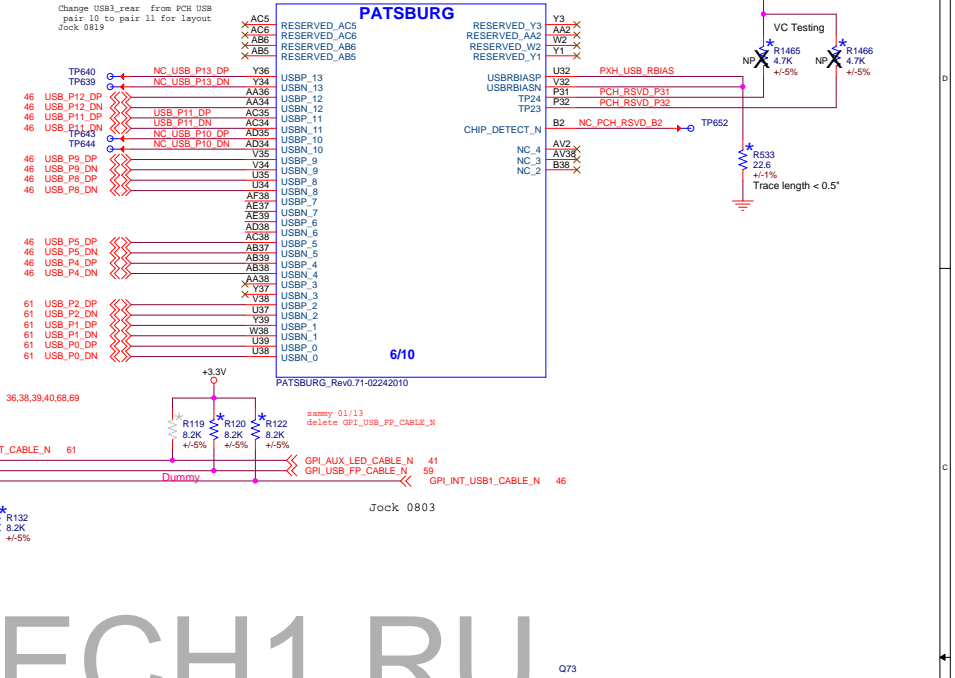


todo: Srin: Check SAS NB\SB
SAS Ports 0&1 @ 6GB/s
SAS Ports 2-5 @ 3GB/s



U_PCH

PATSBURG

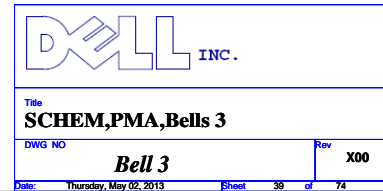


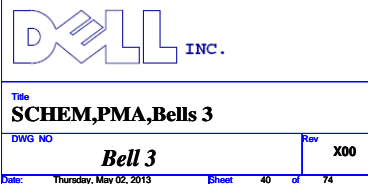
Via spacing (center to center)	Trace spacing (edge to edge)	Trace coupling length	Decoupling Cap?
>=26mil	>=3h (stripline) >=3h (microstrip)	<=0.3"	duf/decap Required

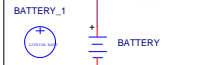
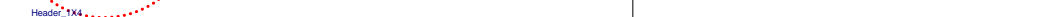
SGPIO Pull Ups pg. 88
Place PU within 2" from PBG



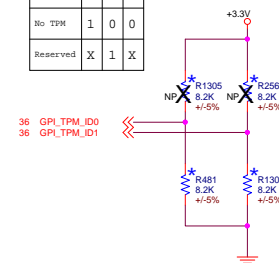
PATSBURG

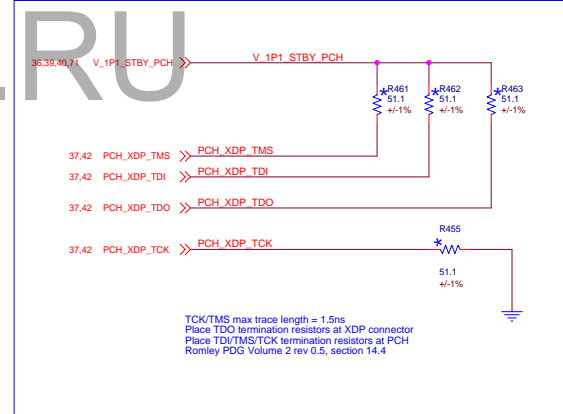
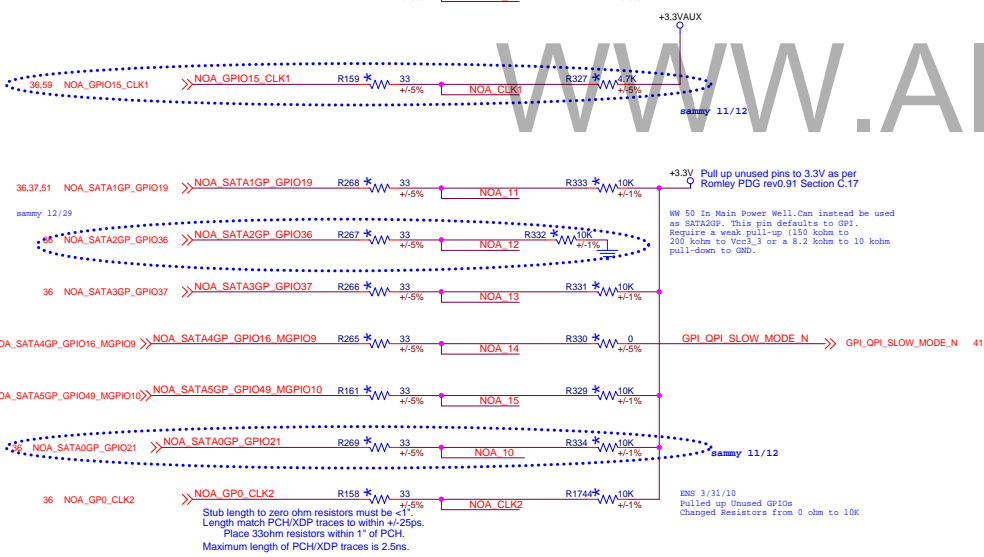
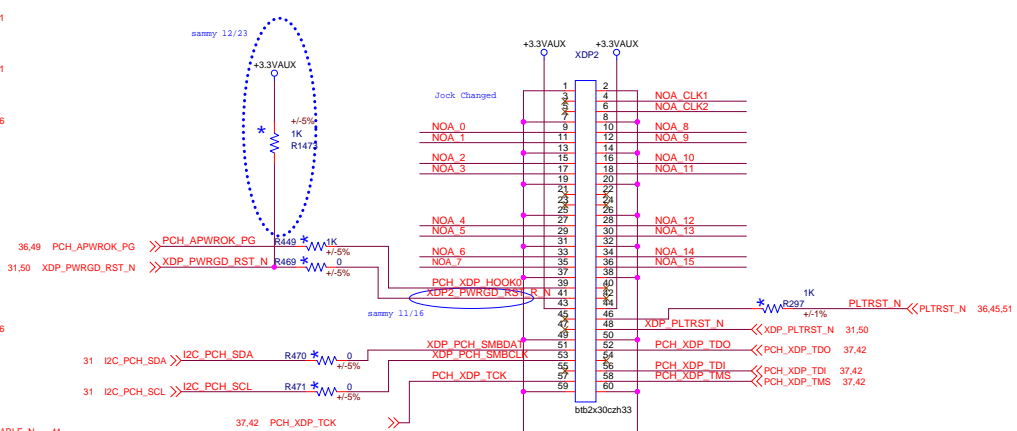
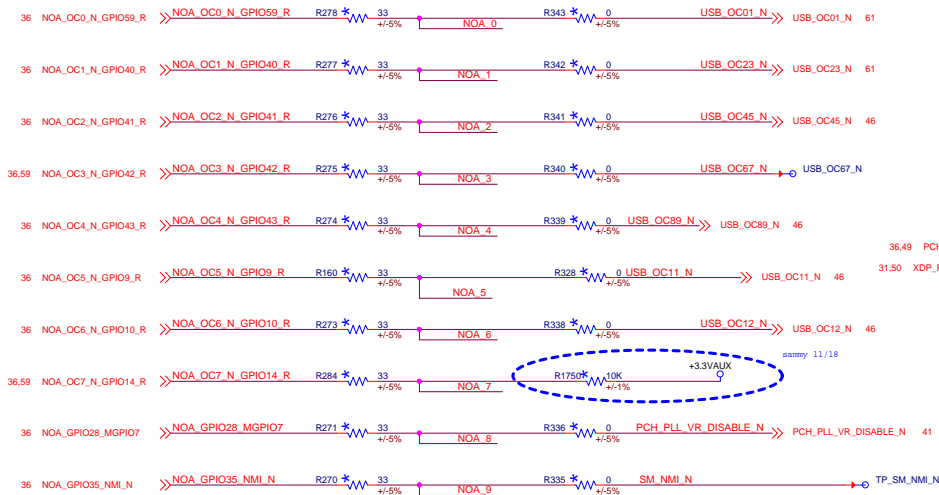







DWG NO	<i>Bell 3</i>	Rev	X00
Date:	Thursday, May 02, 2013	Sheet	41 of 74

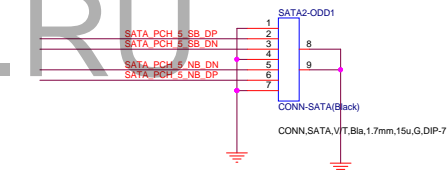
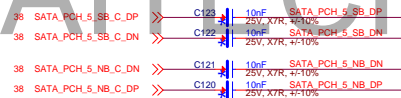
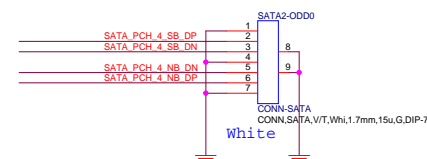
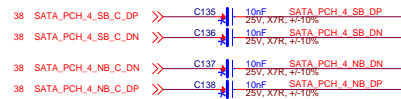
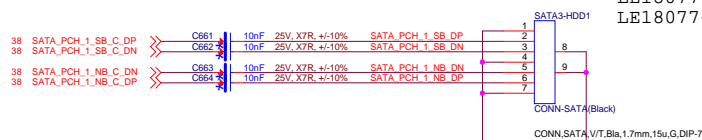
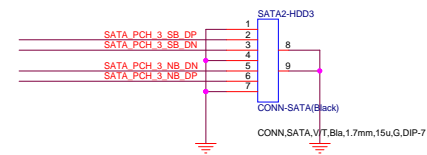
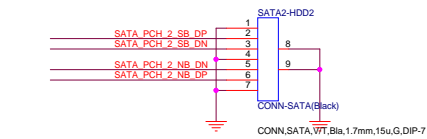
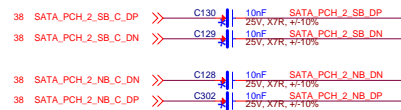
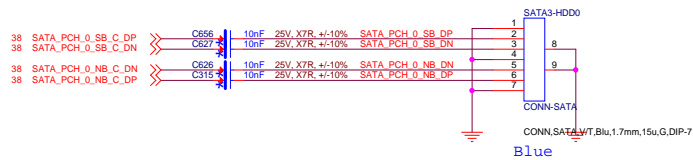




Place series Res by PCH. (See PDG)

WWW.AITECH1.RU

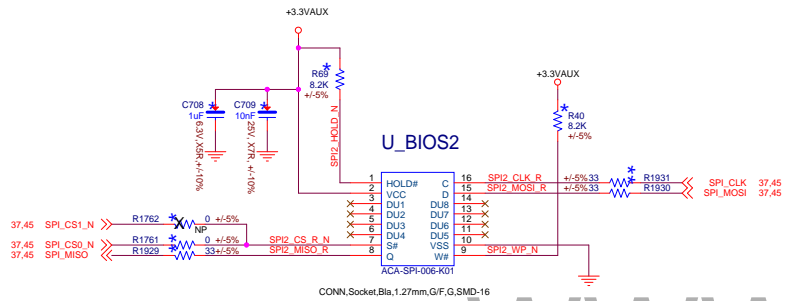
 INC.	
Title SCHEM,PMA,Bells 3	
DWG NO Bell 3	Rev X00
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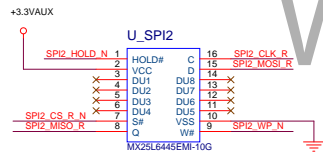
SATA 6G connector
LE18077-A50D-4F
LE18077-W50D-4F
LE18077-Z50D-4F

WWW.AITECH1.RU

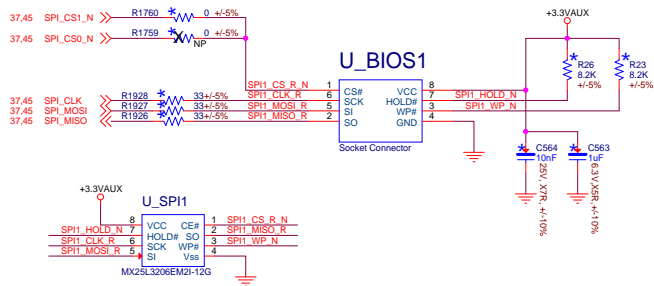
sammy 11/12
Delete ESATA feature(connector,redriver and all related components)



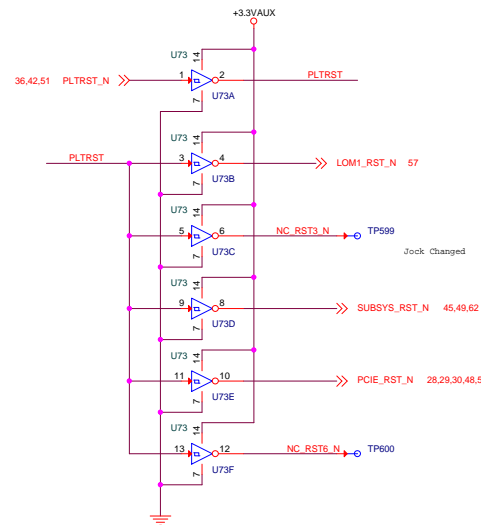
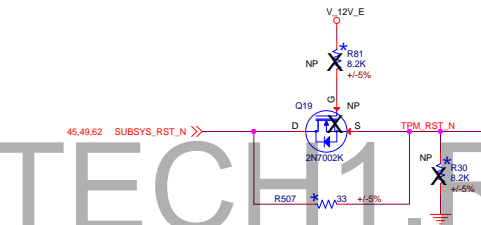
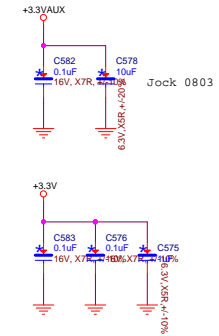
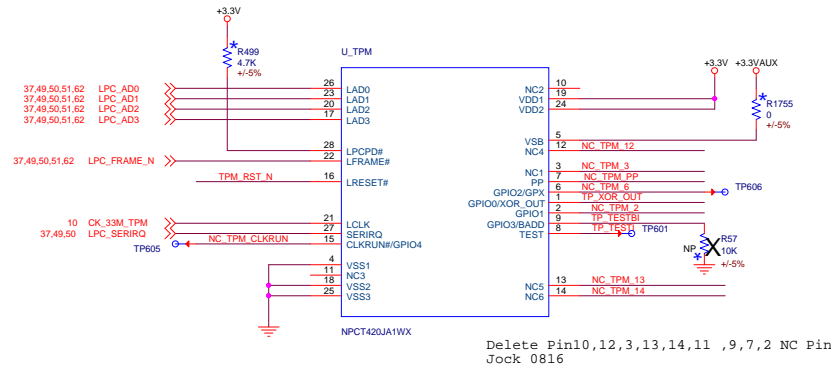
CONN.Socket,Bla,1,27mm,G/F,G.SMD-16

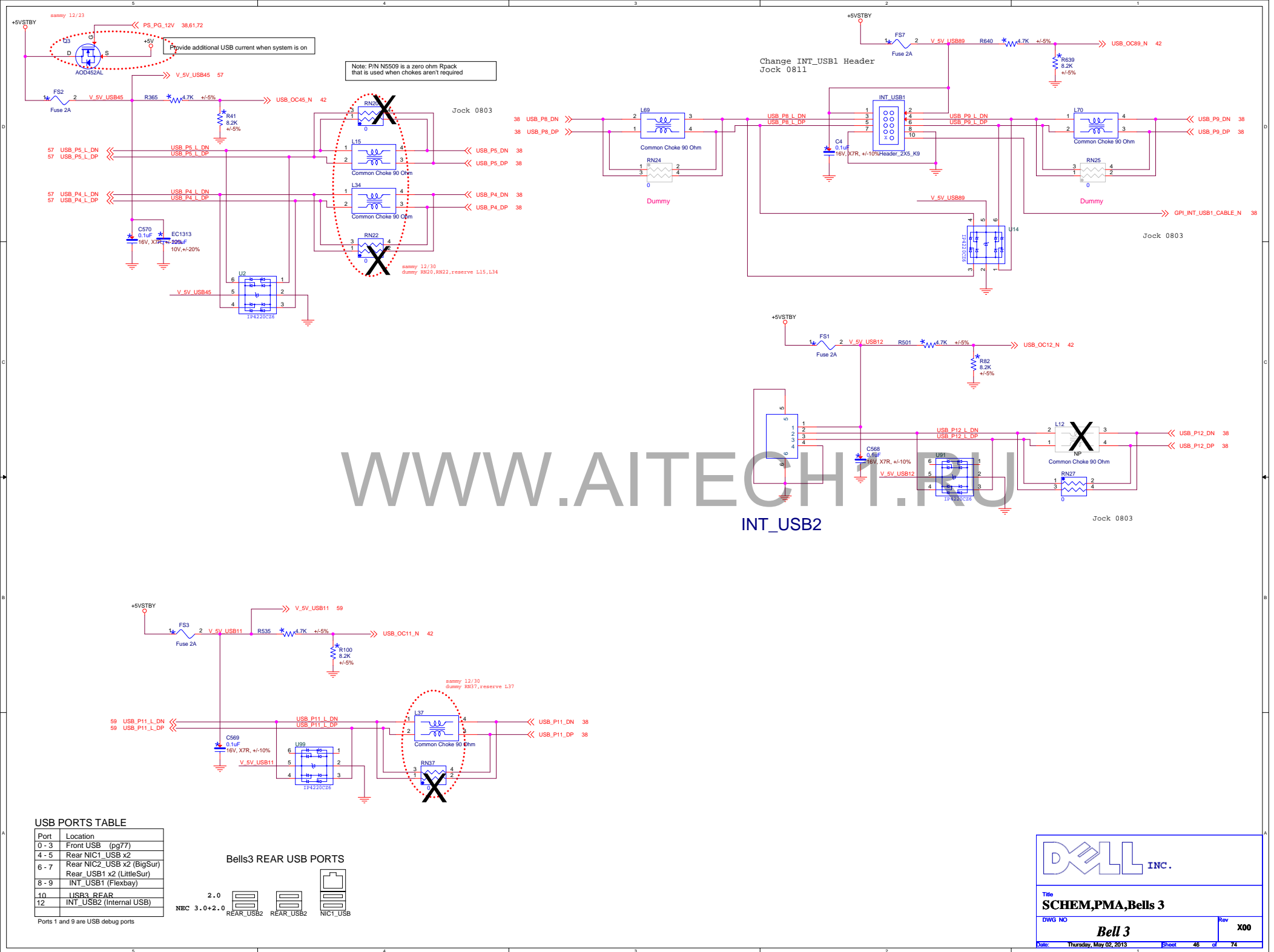


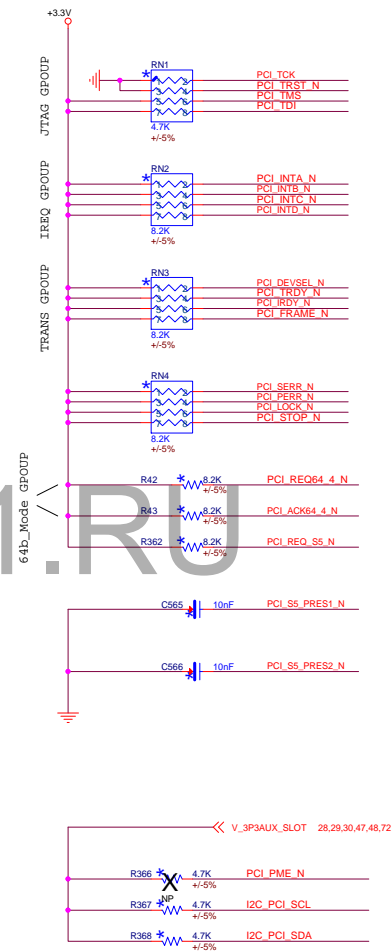
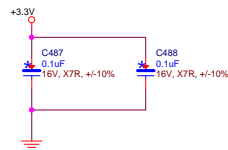
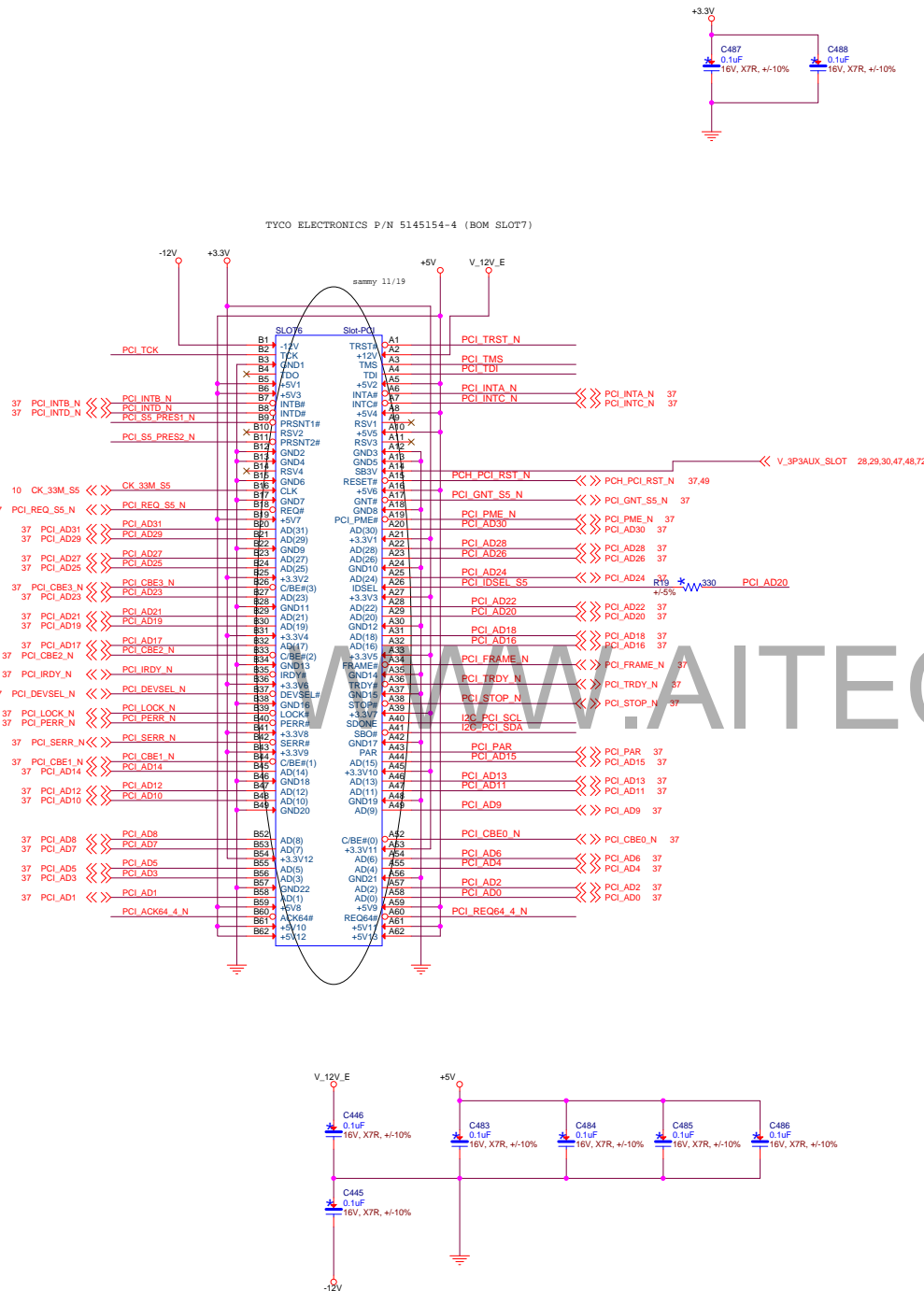
SPI FLASH



Blank 32Mb PN: U141D
Blank 16Mb PN: TT638
SOIC Socket PN: FY6WX



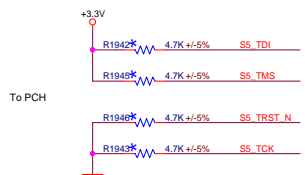
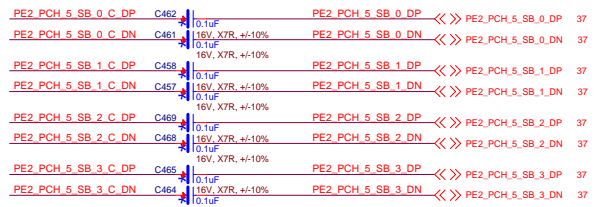
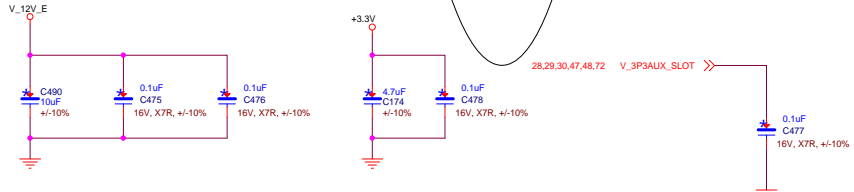
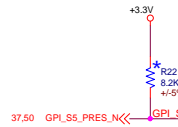
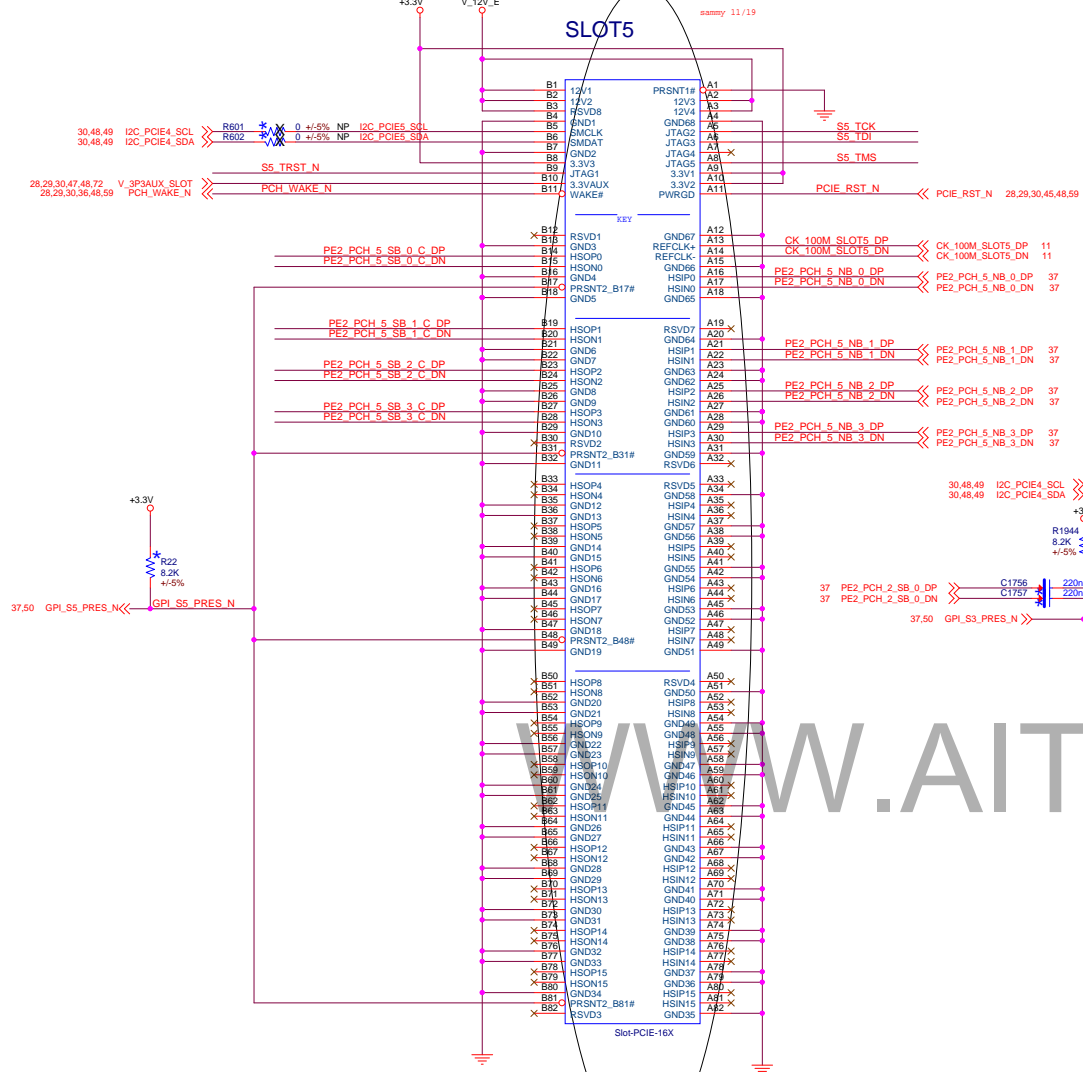




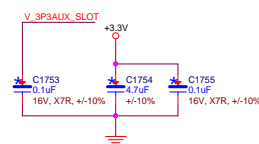
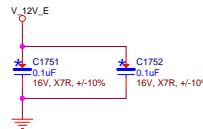
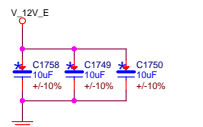
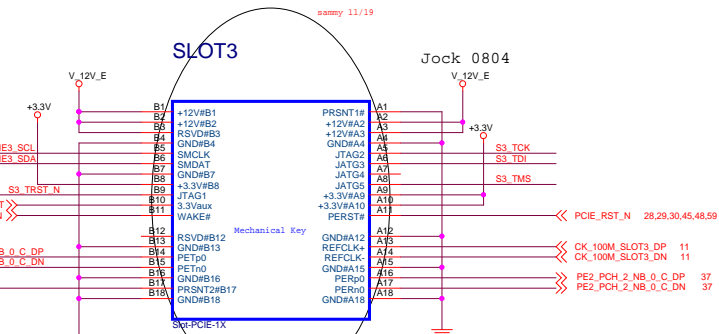
PCI32 SLOT

Title SCHEM,PMA,Bells 3	
DWG NO Bell 3	Rev X00
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SLOT5



SLOT3



PCIE. SLOTS 3.5

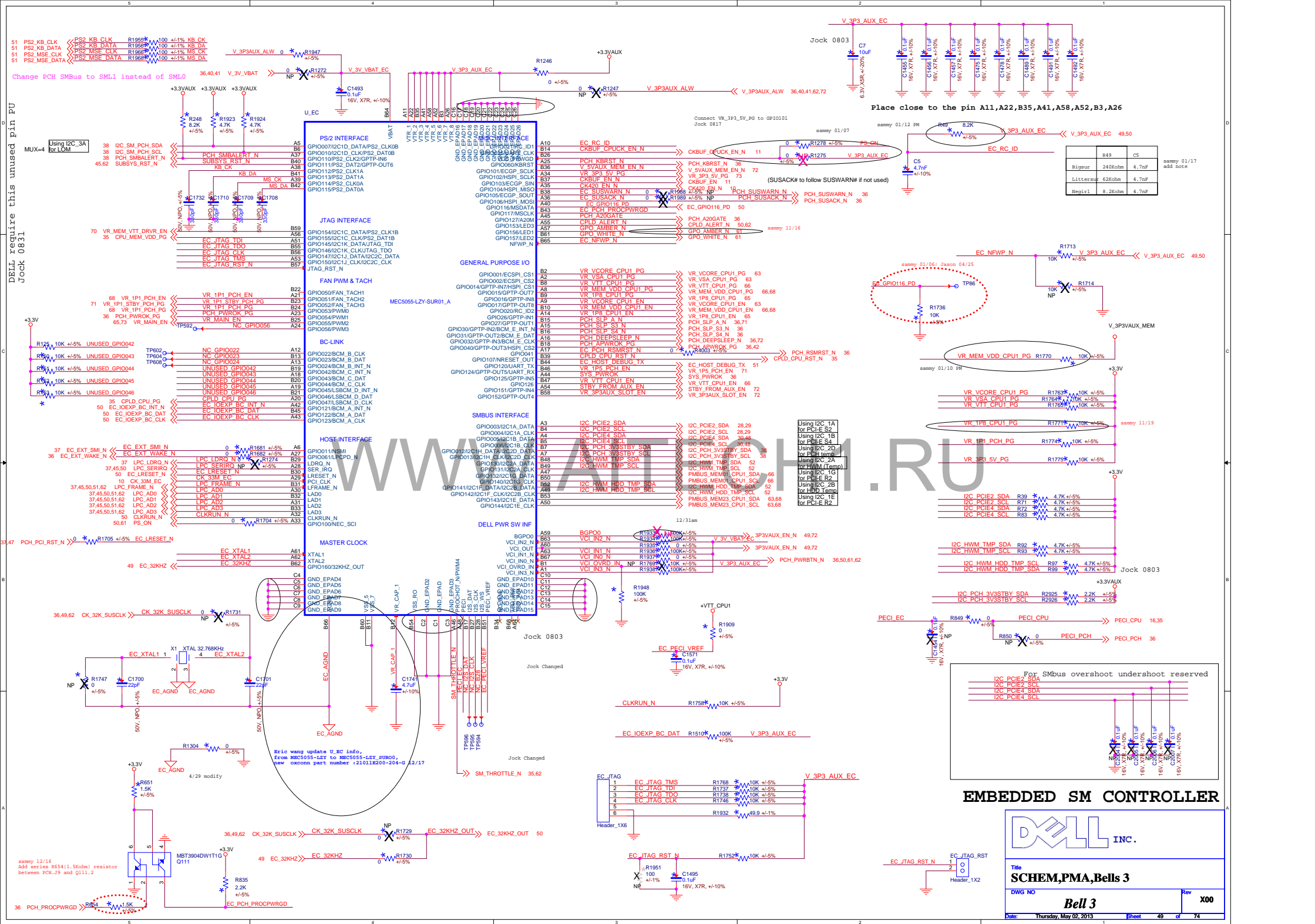


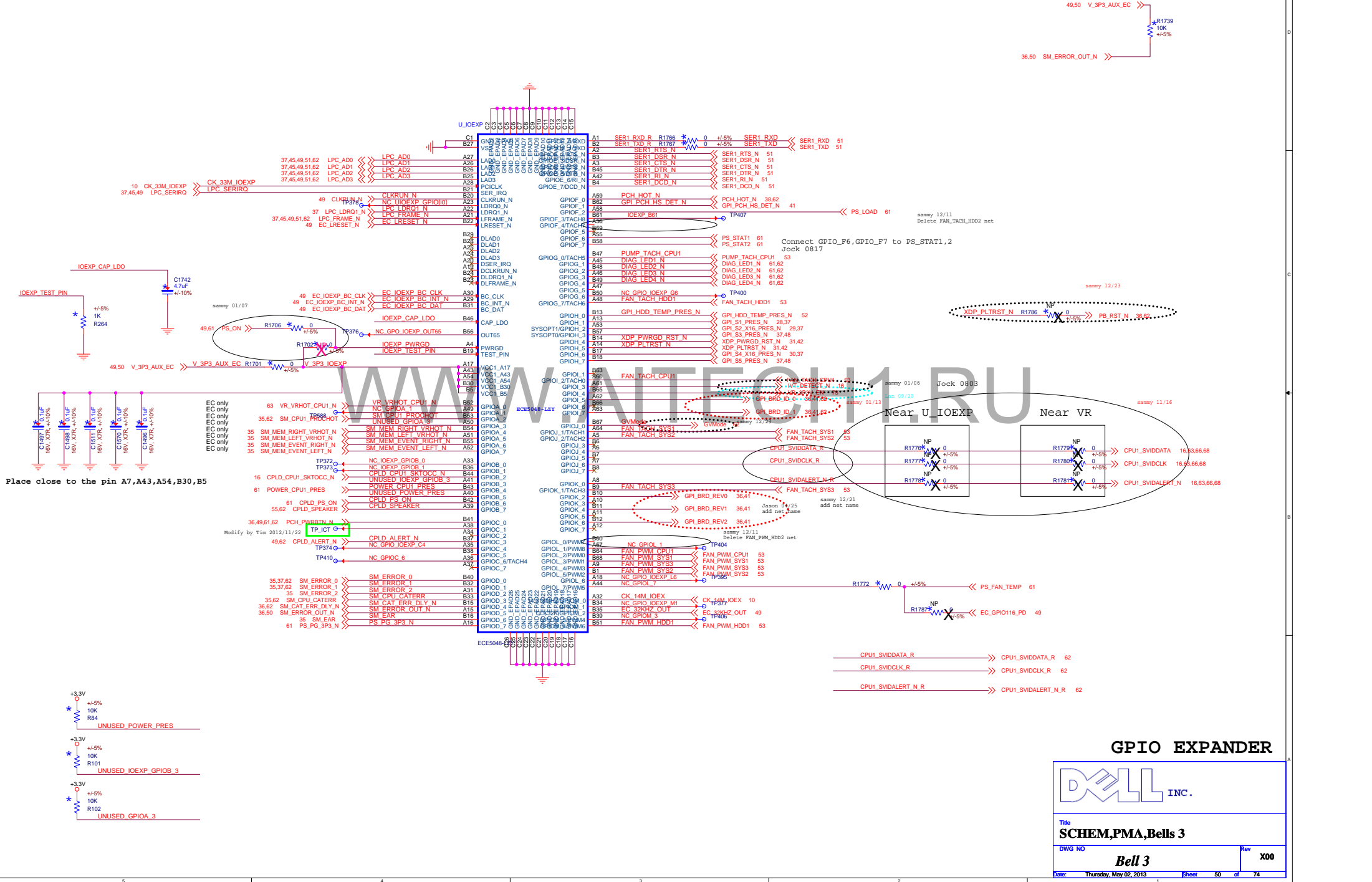
Title
SCHEM,PMA,Bells 3

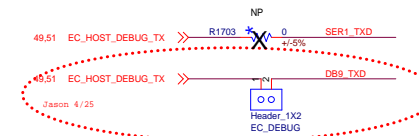
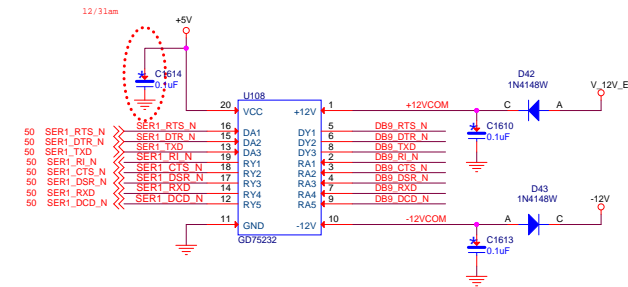
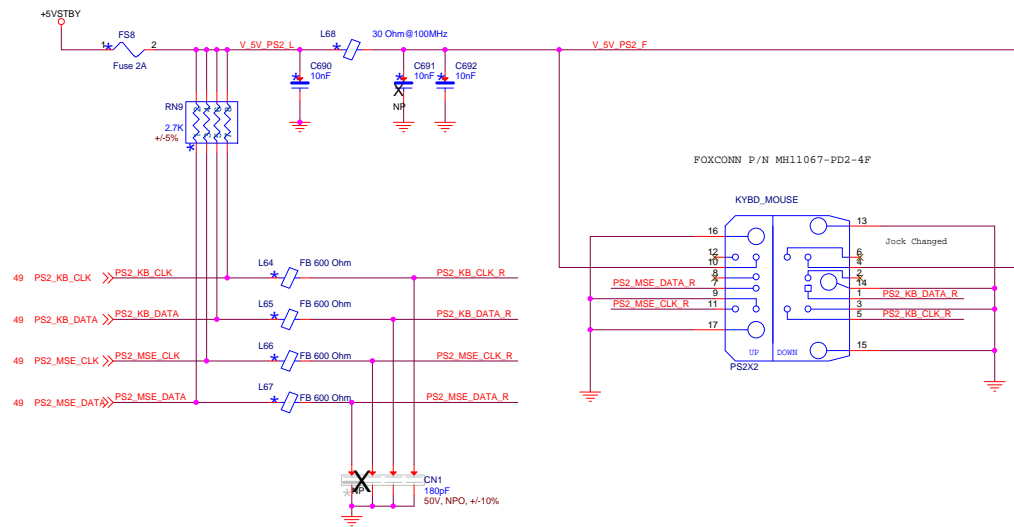
DWG NO
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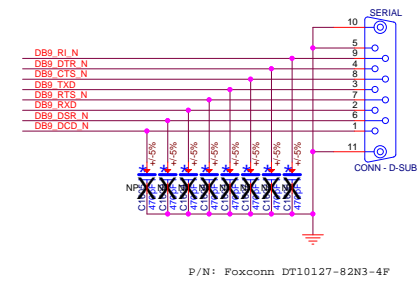
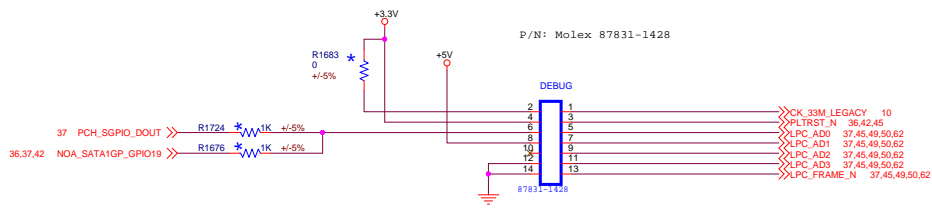




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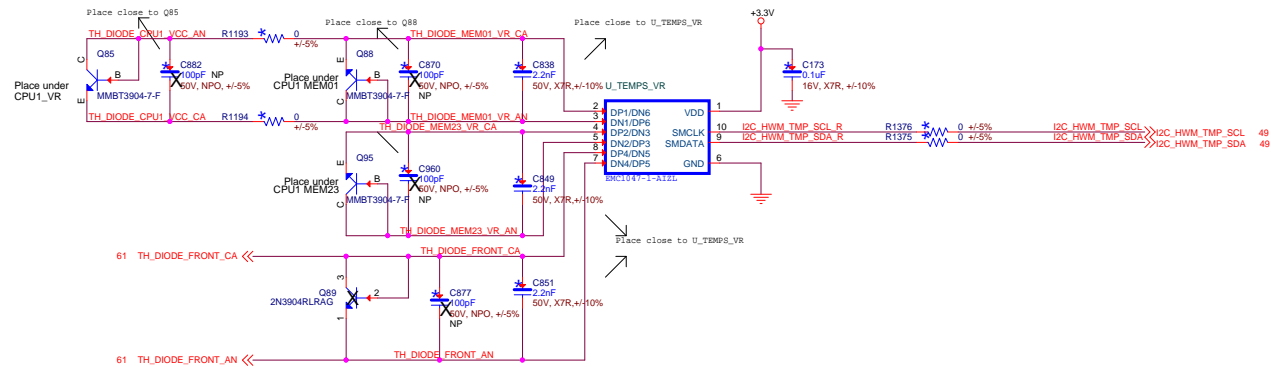
LEGACY IO Connector

see BigSur pg53 for boot bios strapping options
also acts as LPC Debug connector
populate



KYBD\MOUSE, SERIAL

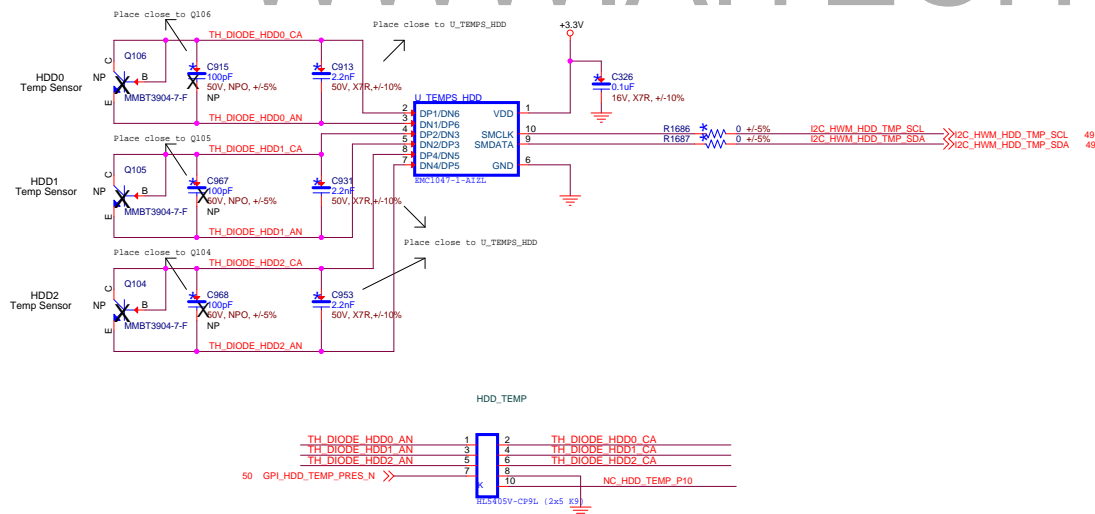
DELL INC.	
Title SCHEM,PMA,Bells 3	
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Date Thursday, May 02, 2013	Sheet 51 of 74



sammy 11/12

Ambient
Temp Sensor

WWW.AITECH1.RU



Header&Socket 34064WH00-600-G
Connector,HL5405V-CP9L,Shrouded Header,9,DIP,LCP,2mm,15u",Black,G

HW MONITOR

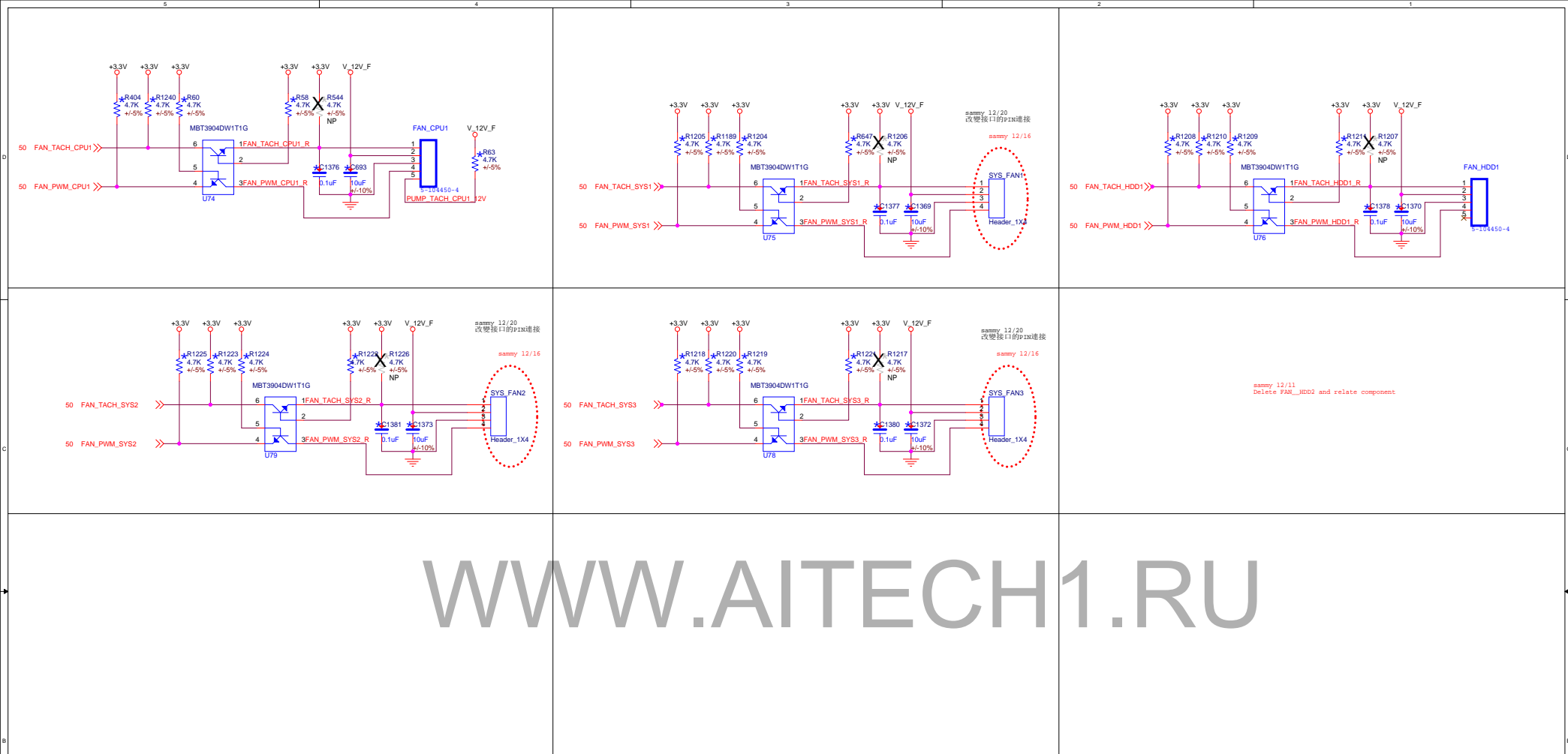


Title
SCHEM,PMA,Bells 3

DWG NO
Bell 3

Rev
X00

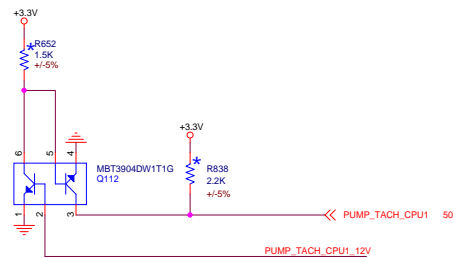
Date: Thursday, May 02, 2013 Sheet 52 of 74



WWW.AITECH1.RU

Fan Matrix

	S048 PWM TACH 0	S048 PWM TACH 1	S048 PWM TACH 2	S048 PWM TACH 3	S048 PWM TACH 4	S048 PWM TACH 5	S048 PWM TACH 6	S048 PWM TACH 7	S048 PWM TACH 8
Latitude	CPU1 Fan	CPU2 Fan	MEM RIGHT FAN	MEM LEFT FAN	FAN_PC01	FAN_PC02	HDD1 FAN	HDD2 FAN	HDD3 FAN
Latitude Lite	CPU1 Fan	CPU2 Fan	MEM RIGHT FAN	MEM LEFT FAN	FAN_PC01	FAN_PC02	HDD1 FAN	HDD2 FAN	HDD3 FAN



FAN CONNECTOR




Title
SCHEM,PMA,Bells 3

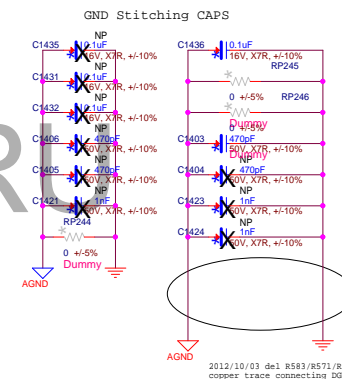
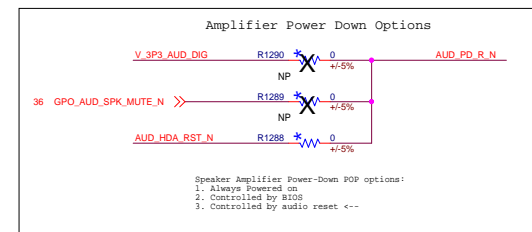
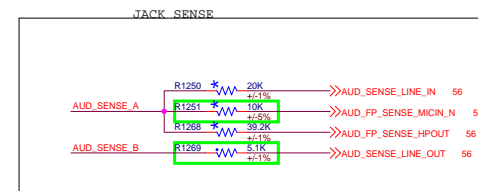
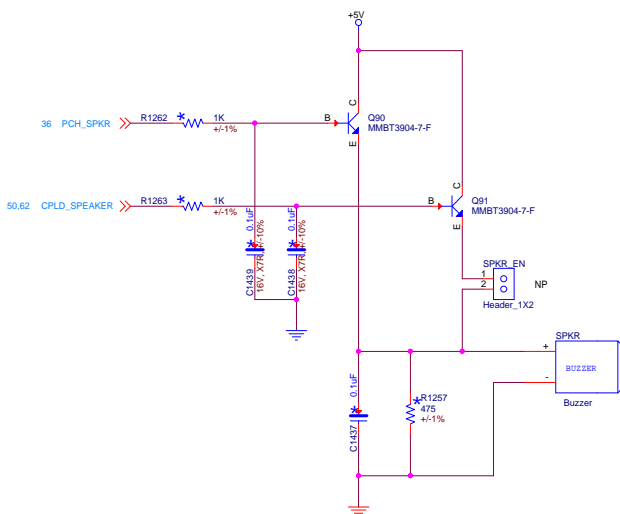
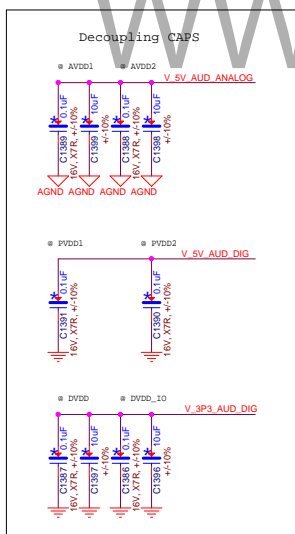
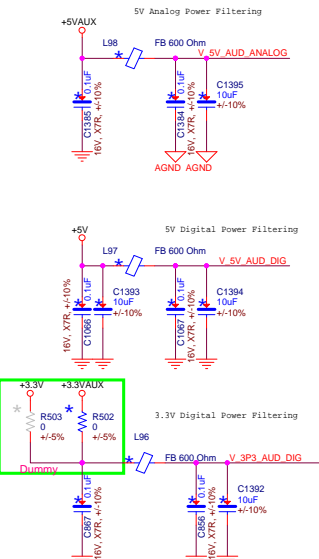
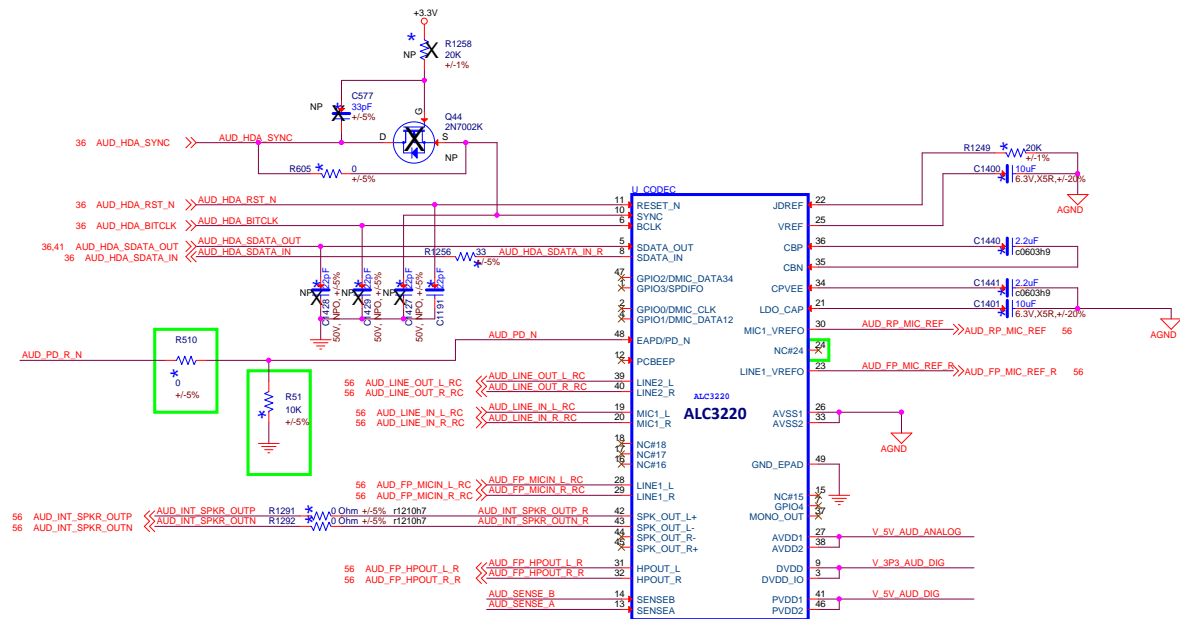
DWG NO
Bell 3

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DWG NO Bell 3	Rev X00
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AUDIO CODEC

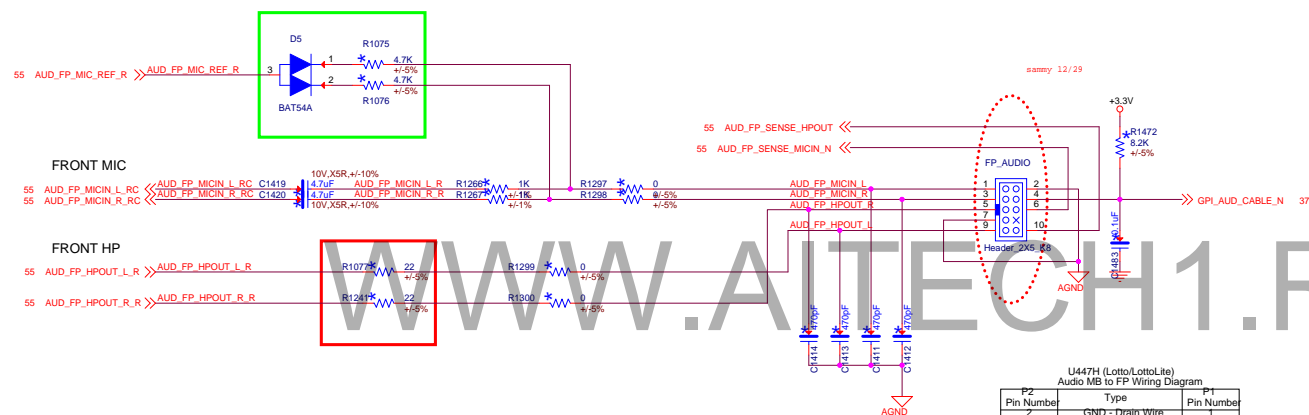


Title
SCHEM,PMA,Bells 3

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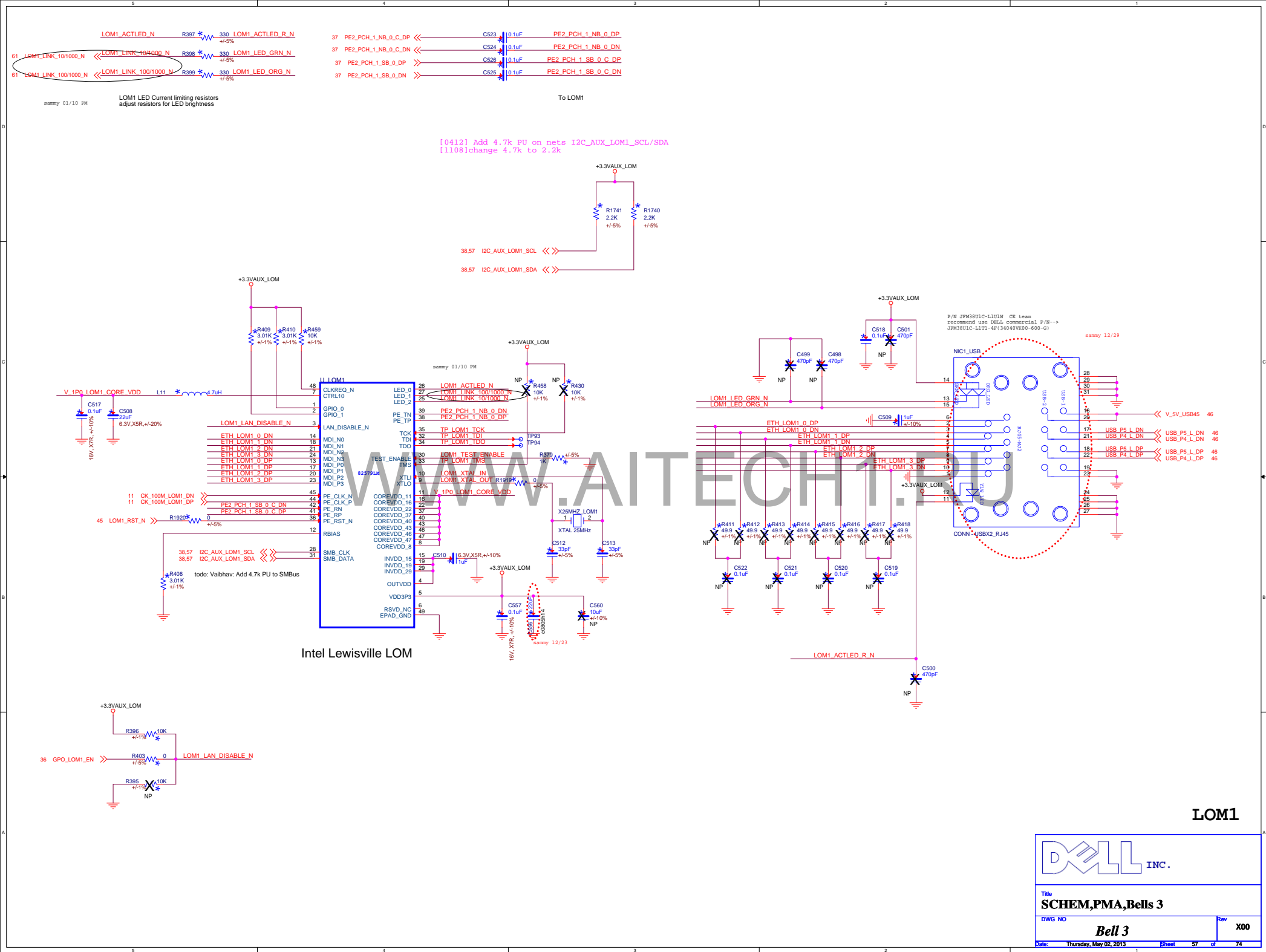
P2 Pin Number	Type	P1 Pin Number
2	GND - Drain Wire	1
9		2
10	Twisted Pair	3
5		4
7	Twisted Pair	5
1		6
7	Twisted Pair	7
3		8
6	Twisted Pair	9
4	Cable Detect	10

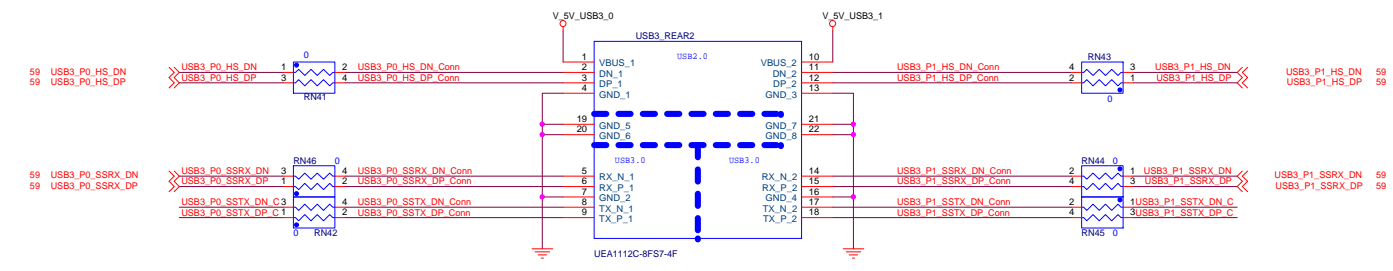
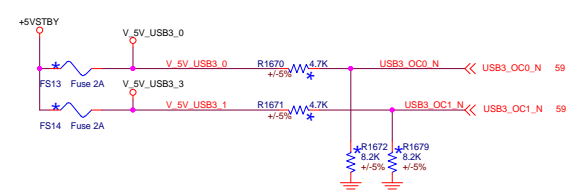
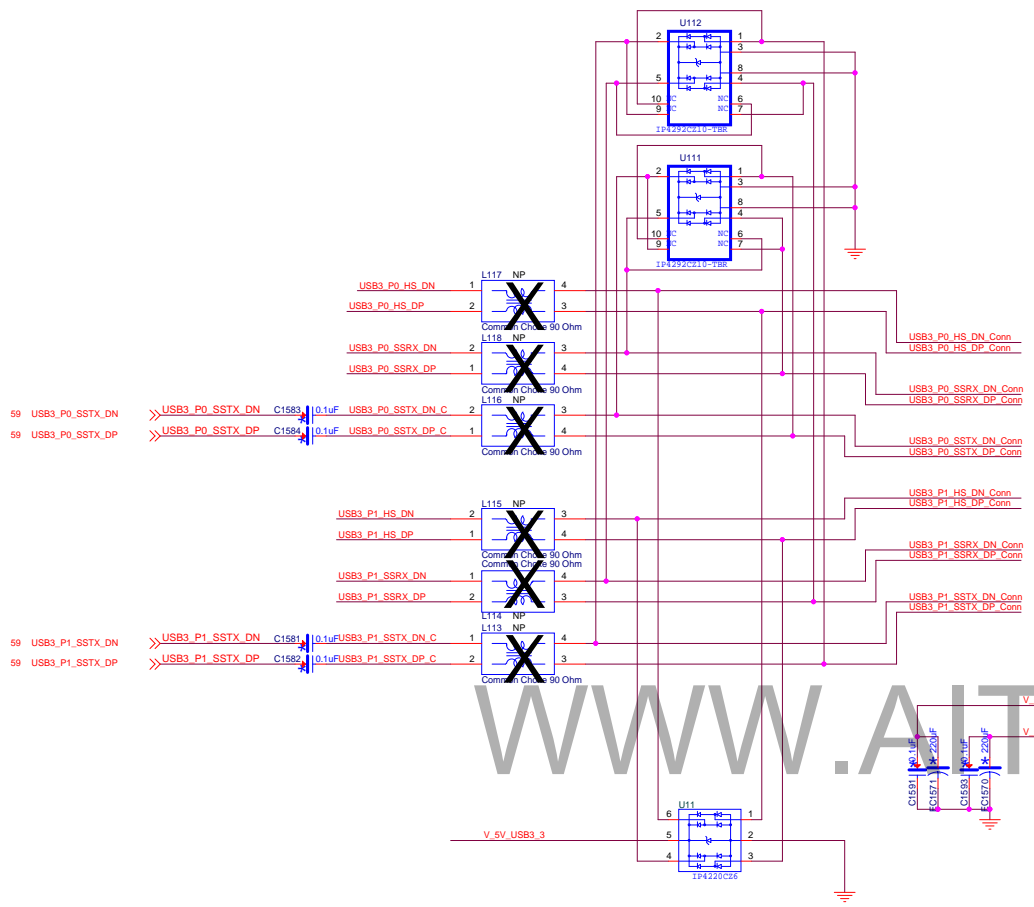


Title
SCHEM,PMA,Bells 3


Bell 3

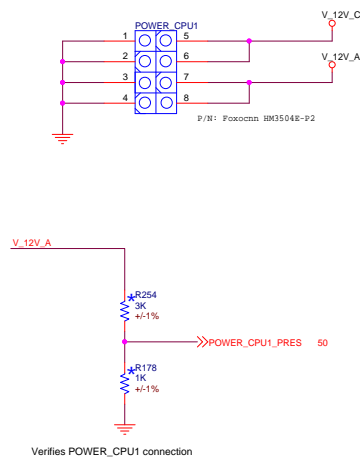
X00



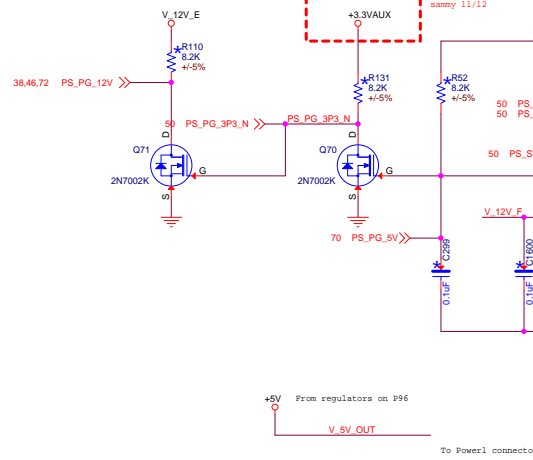


WWW.AITECH1.RU

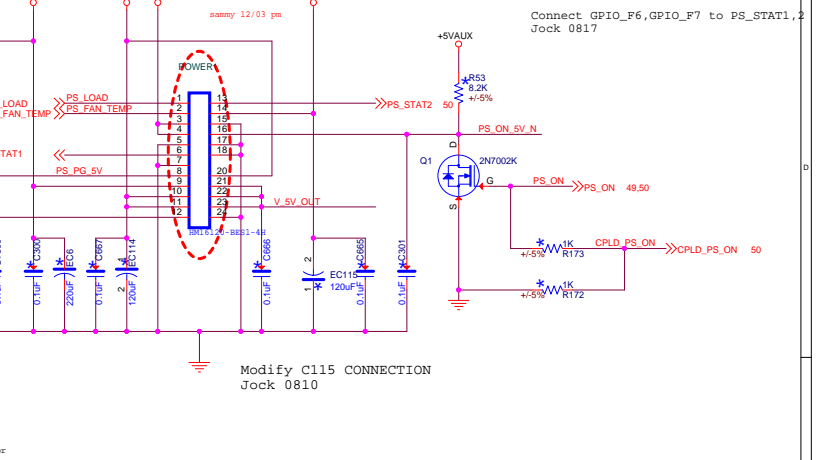
 INC.	
Title SCHEM,PMA,Bells 3	
DWG NO Bell 3	Rev X00
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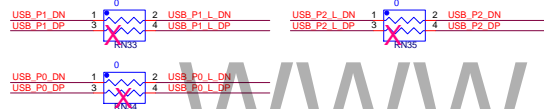
Note: P/N N5509 is a zero ohm Rpack that is used when chokes aren't required



Do not populate when using Lotto wiring harness
Note: Connect P3&4 to +12V, P13 to GND, and short these resistors in the next board revision to support new power supply pinout

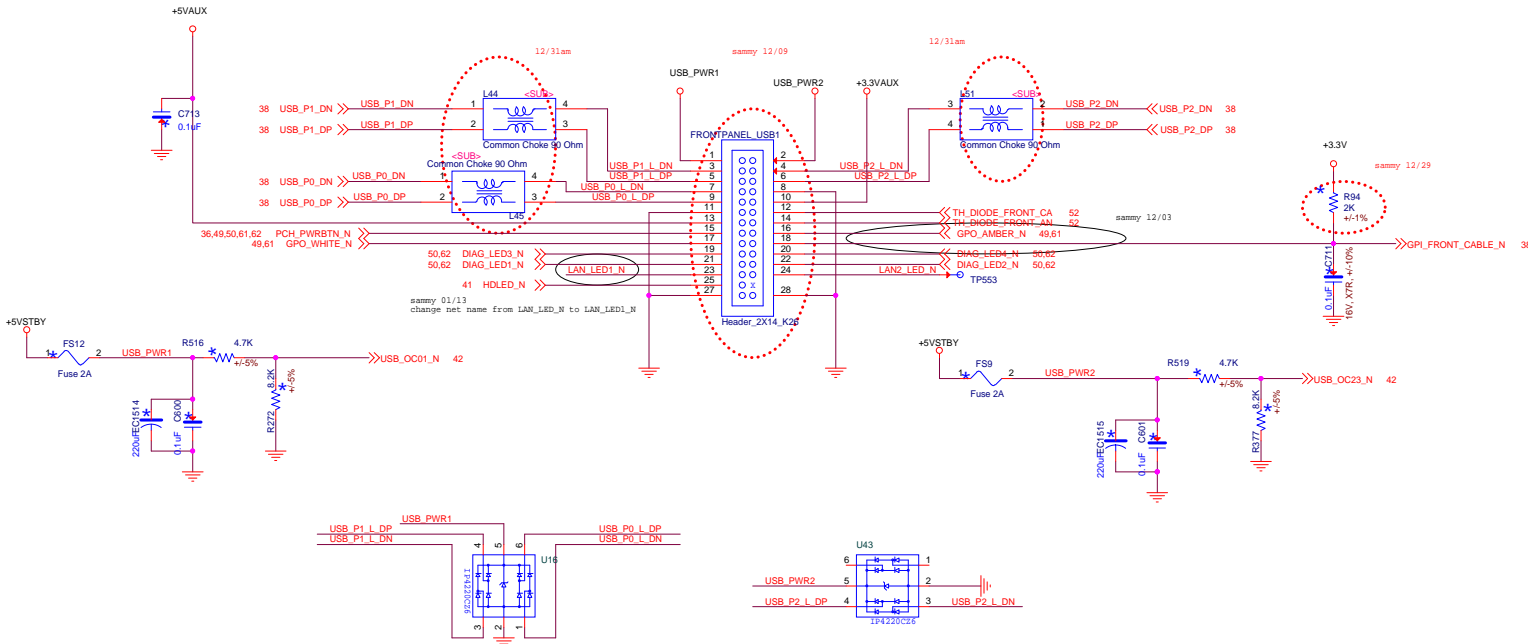


IC: 74VHC1008, 80T353-5, AND

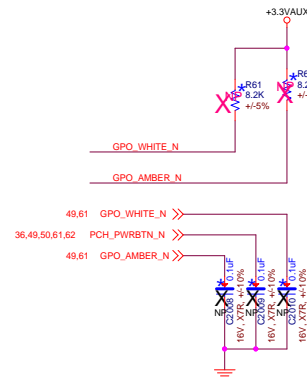


Jock 0803

WWW.AITECH1.RU



sammy 12/16



POWER, FRONT PANEL

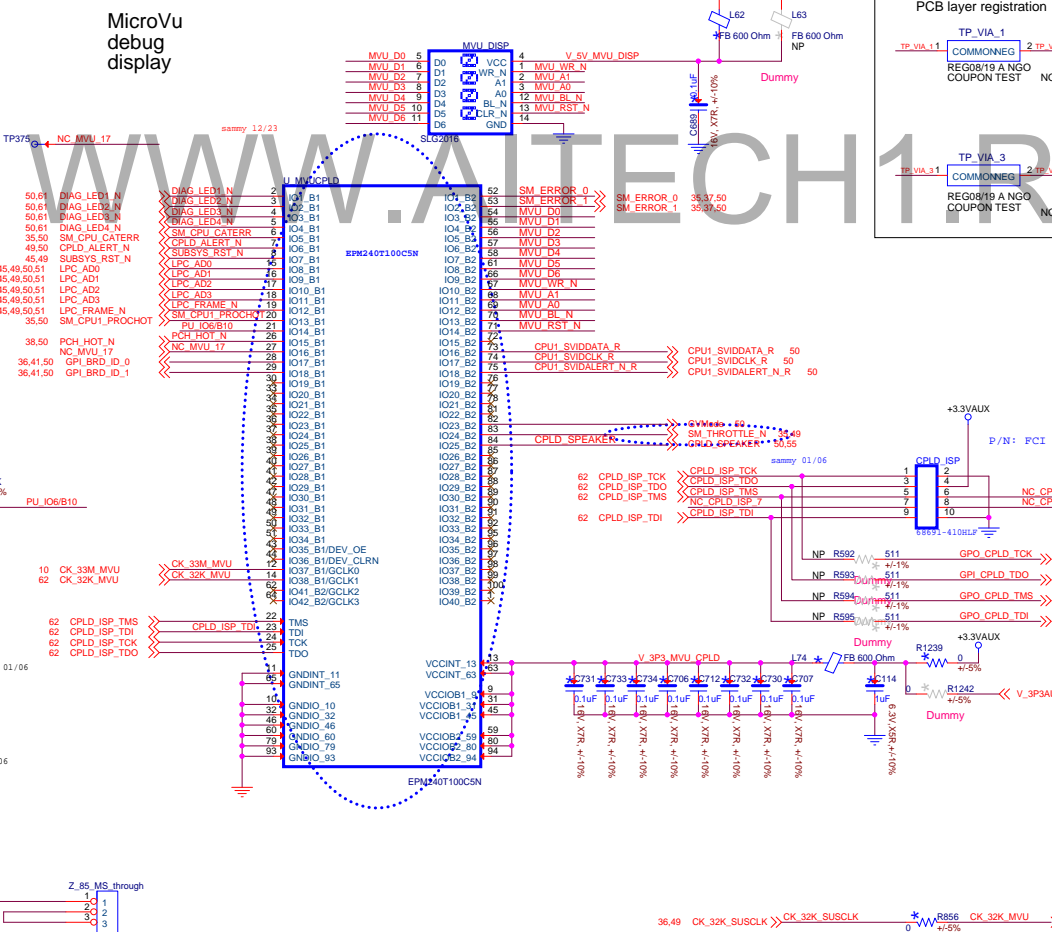
DELL INC.


Title
SCHEM,PMA,Bells 3

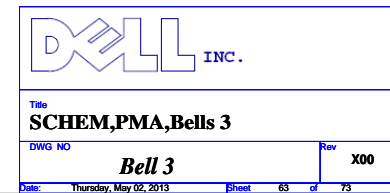
DWG NO
Bell 3

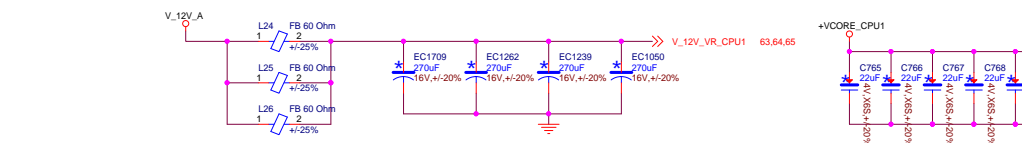
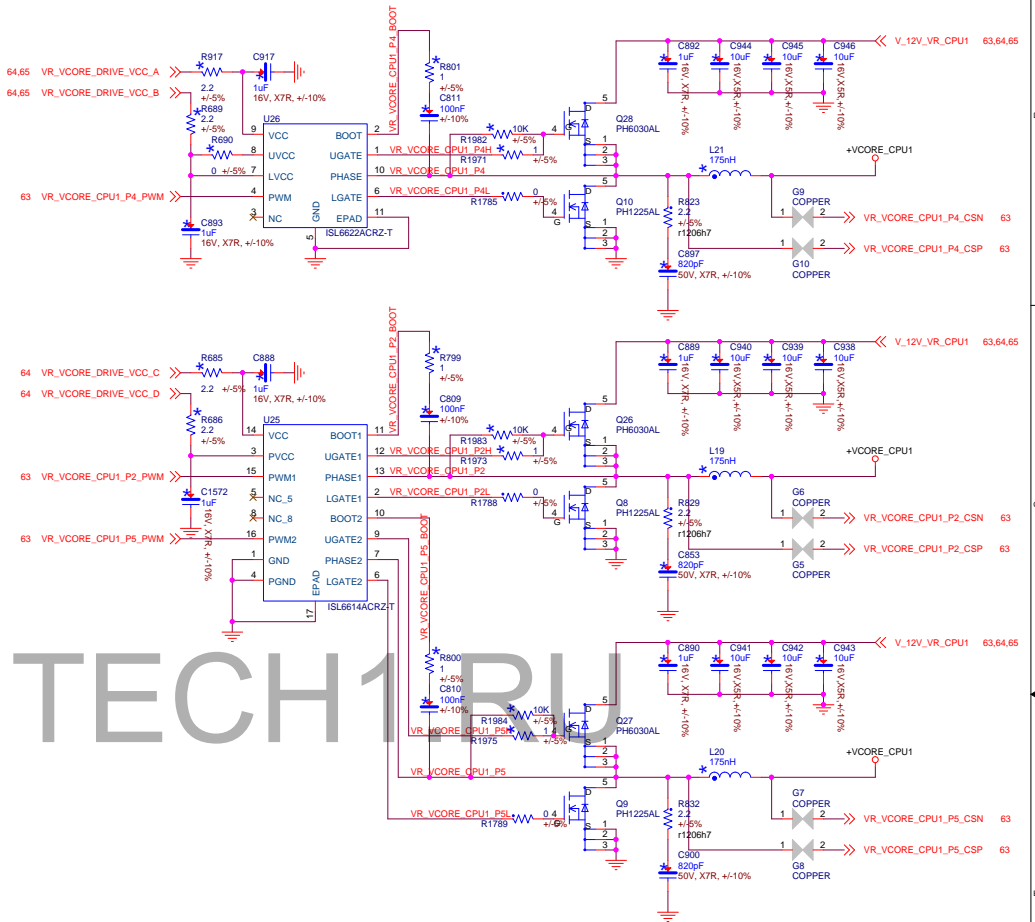
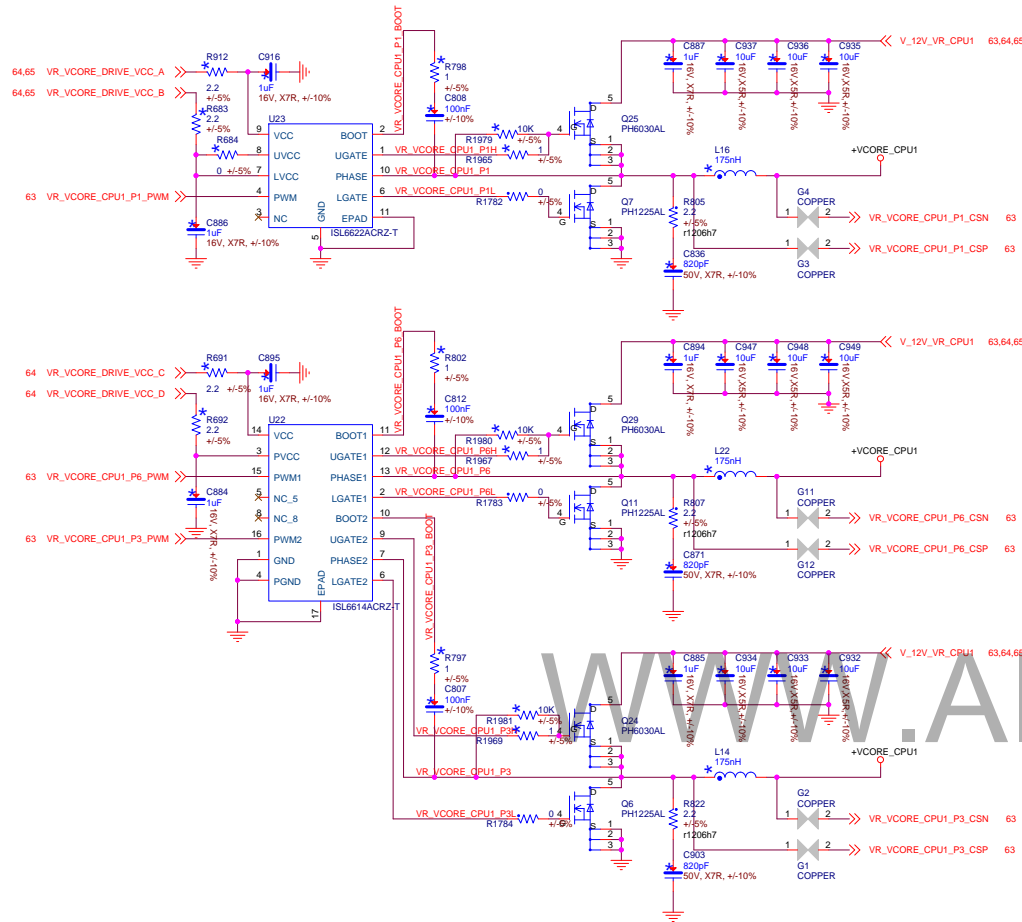
Rev
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Title SCHEM,PMA,Bells 3					
DWG NO				Rev	
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DELL INC.

Title
SCHEM,PMA,Bells 3

DWG NO
Bell 3

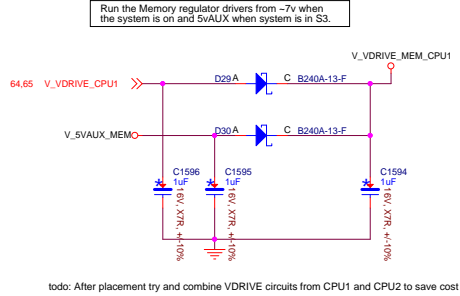
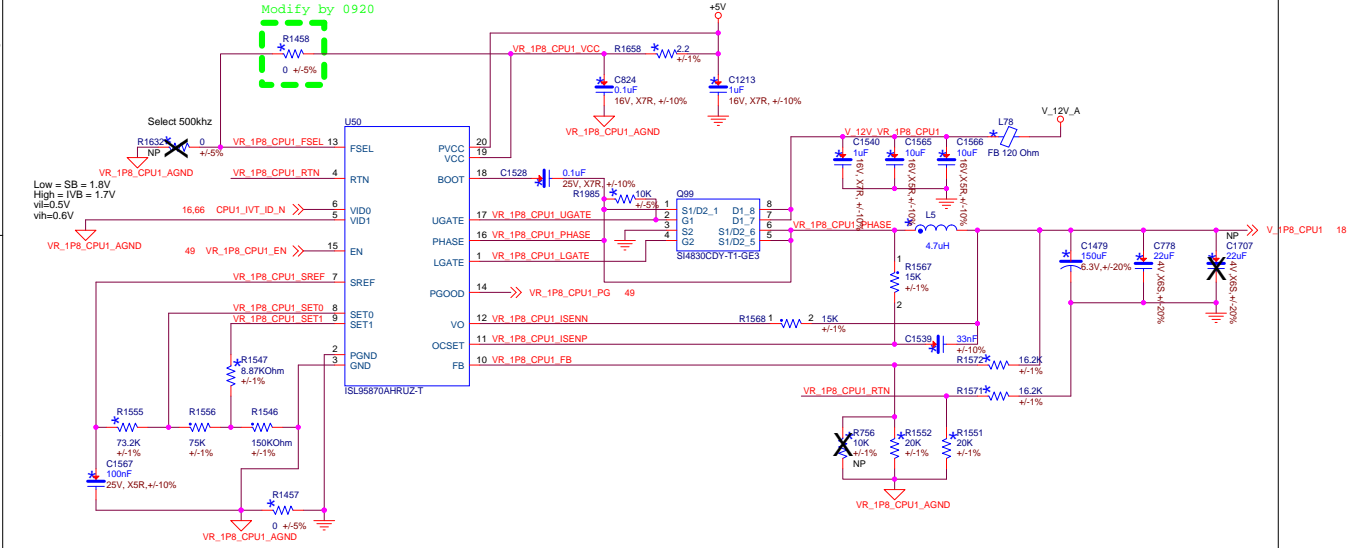
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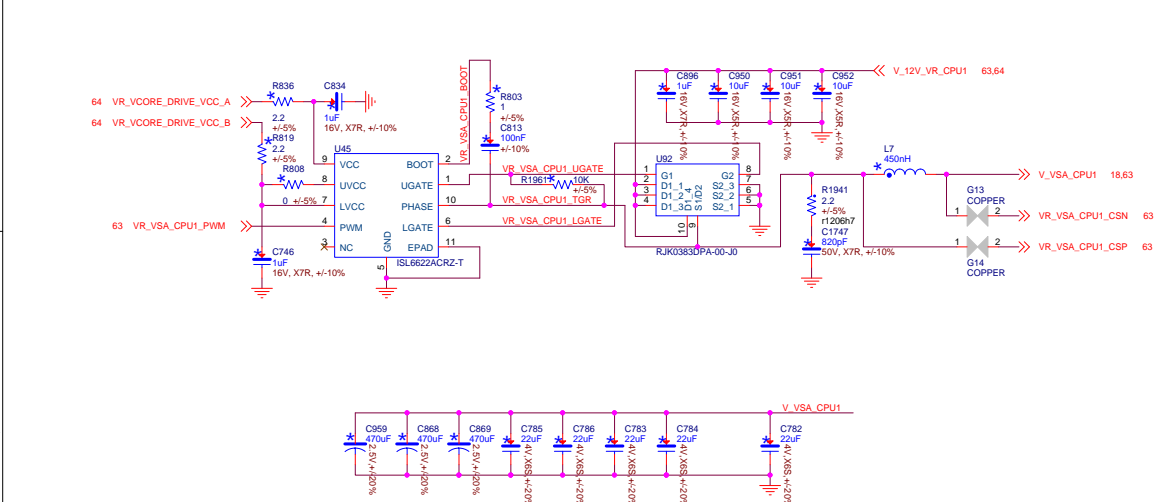
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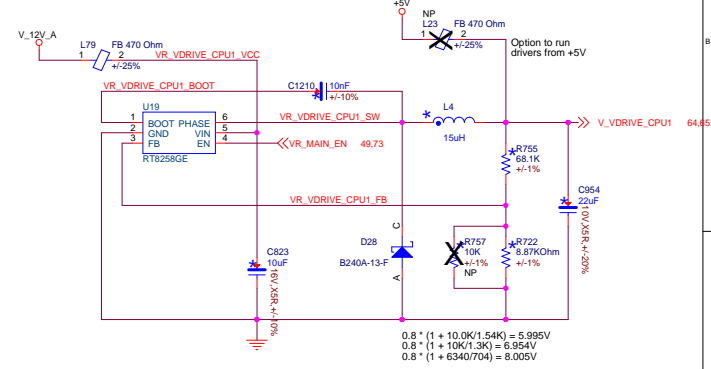
Output	V_1P8_CPU1
Destination	CPU1 PLL Voltage
Input	12V
Peak Current	2.5A
Thermal Current	2.0A
Enabled	
Min Current	500mA



Output	V_VSA_CPU1
Destination	CPU1 VSA rail
Input	12V
Peak Current	VSA 20 A/24 A @ 0.85 V
Thermal Current	16A
Enabled	
Min Current	



Output	V_VDRIVE_CPU1
Destination	CPU1 vcore regulator drivers
Input	12V
Peak Current	1.0A
Thermal Current	390mA
Enabled	
Min Current	120mA
Min CDP	1.6A



Title

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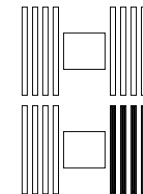
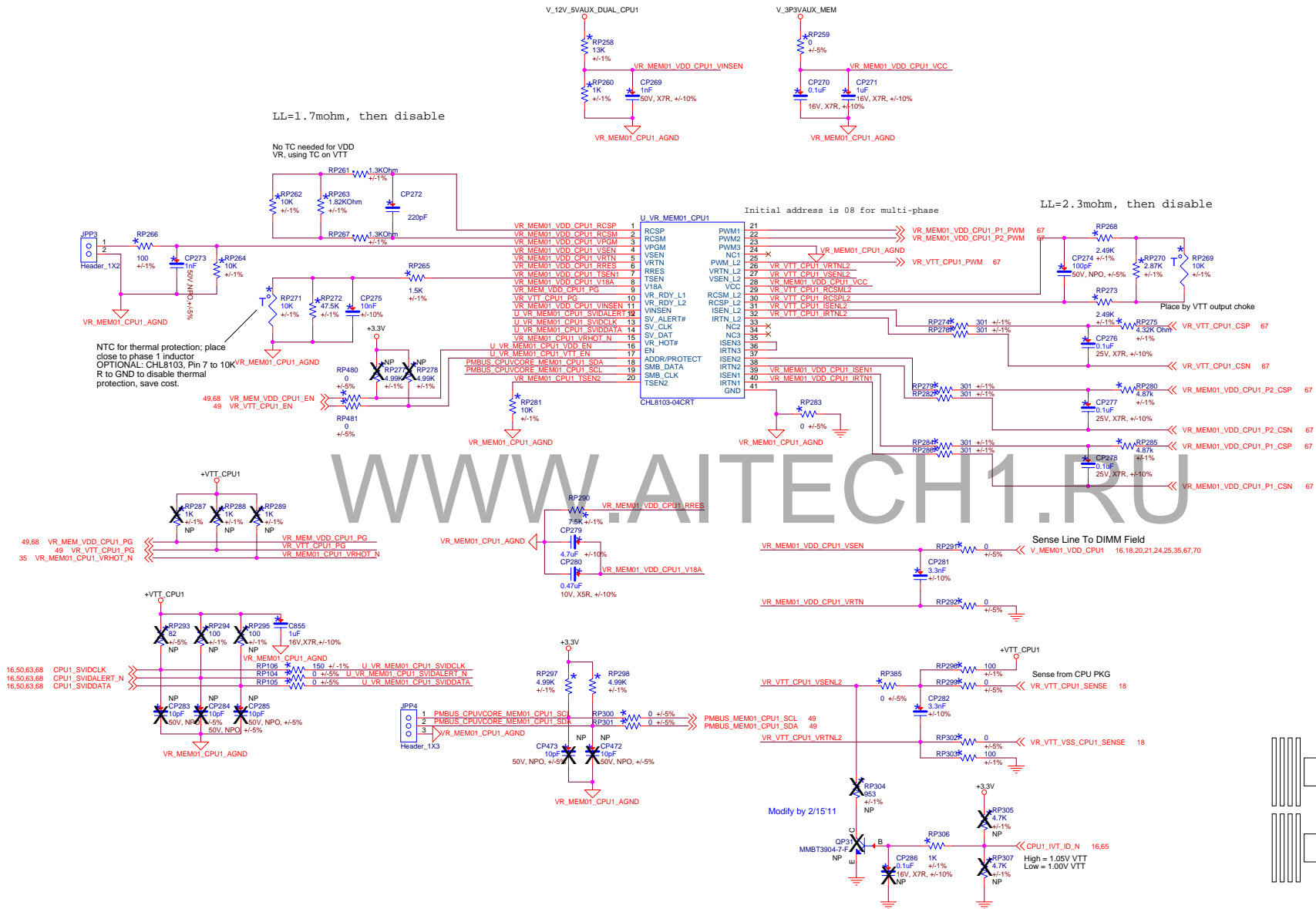
Sheet

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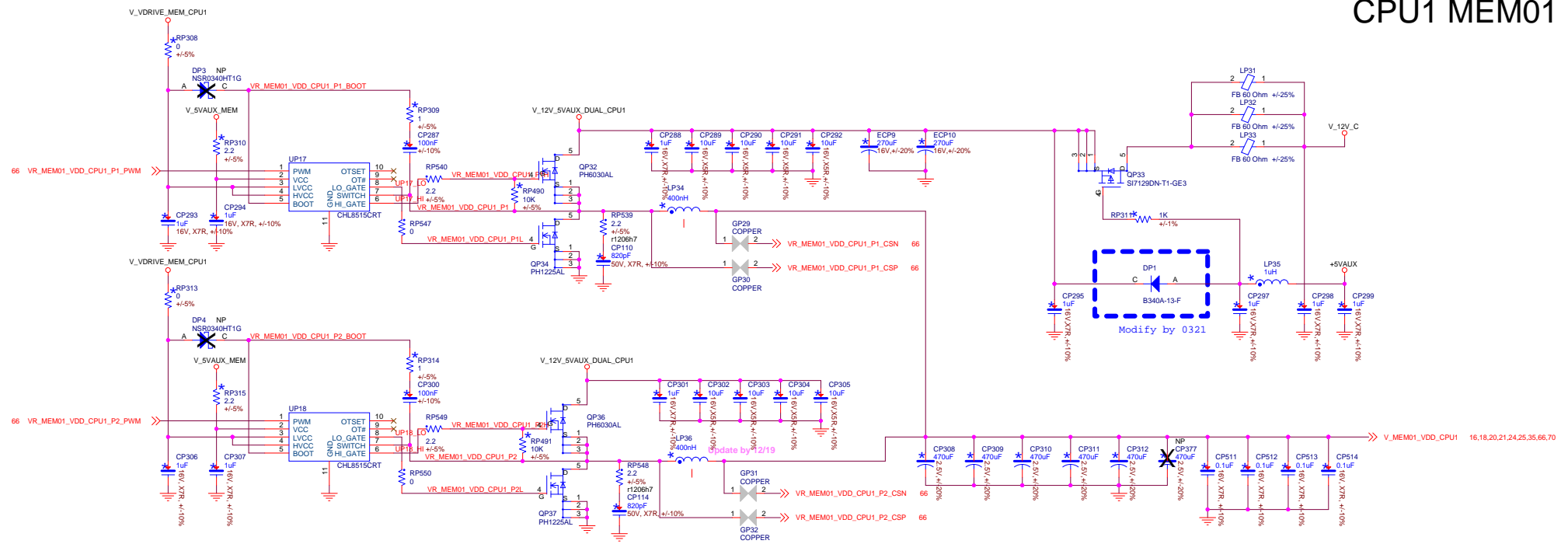
of

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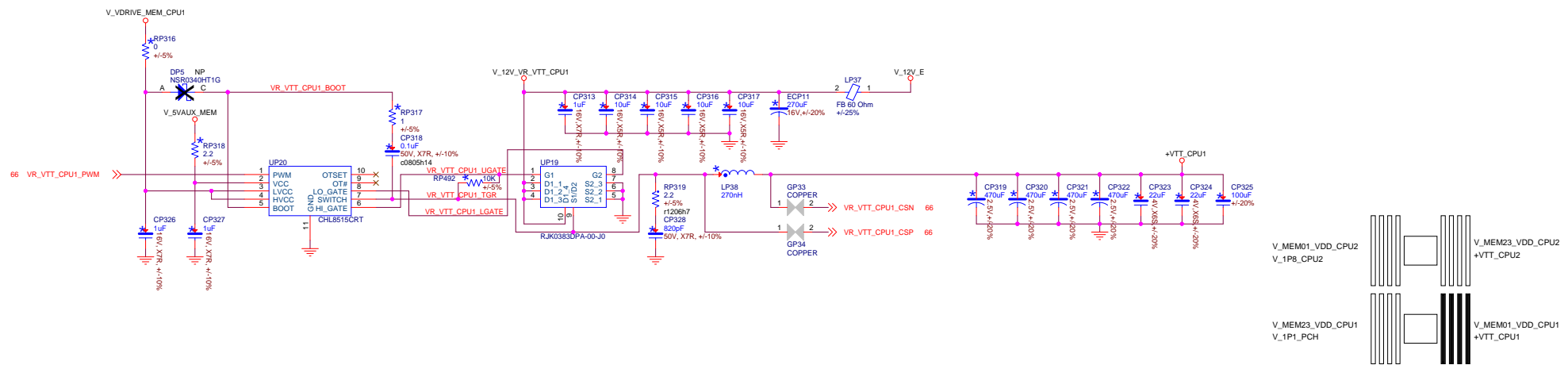
CPU1 MEM01- CHIL CHL8103



CPU1 MEM01



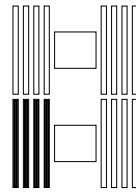
WWW.AITECH1.RU



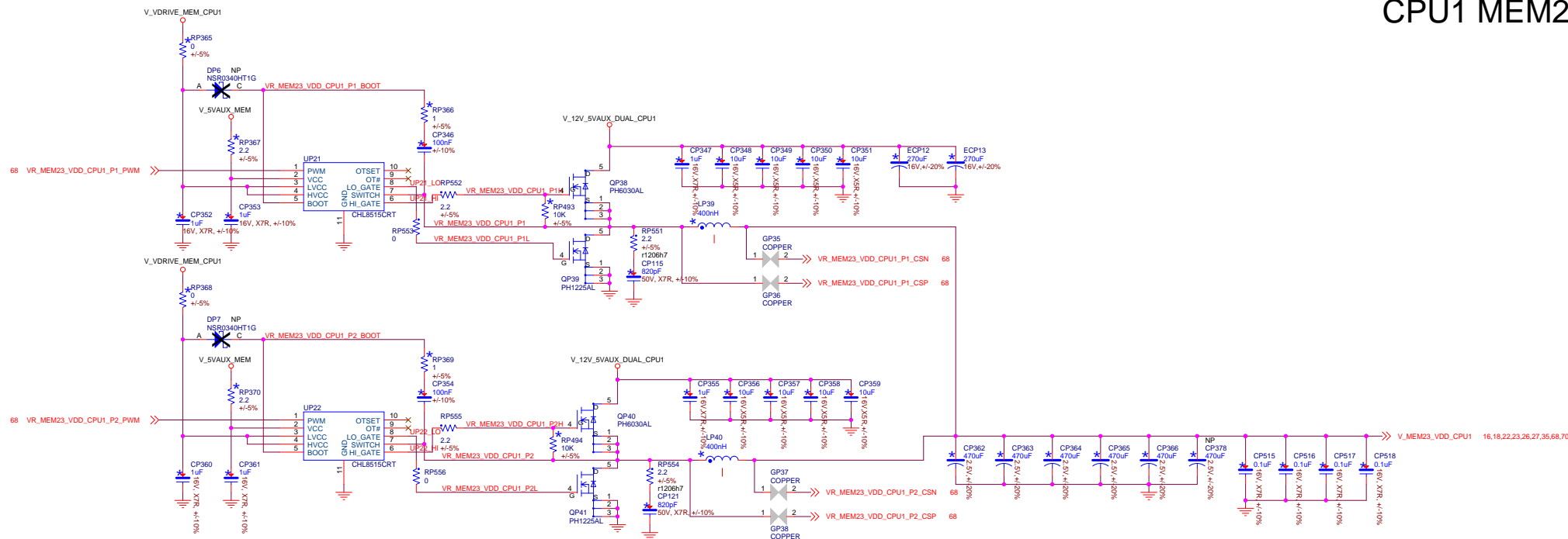
Title
SCHEM, PWA, Bells 3

PN27H

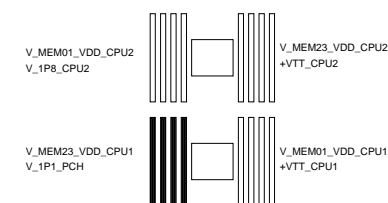
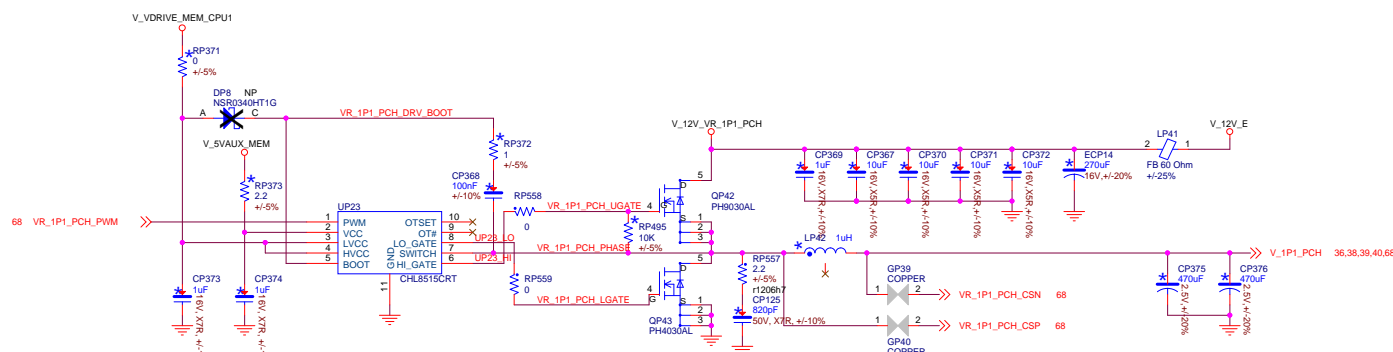
X00

[illegible]

CPU1 MEM23



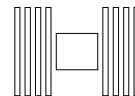
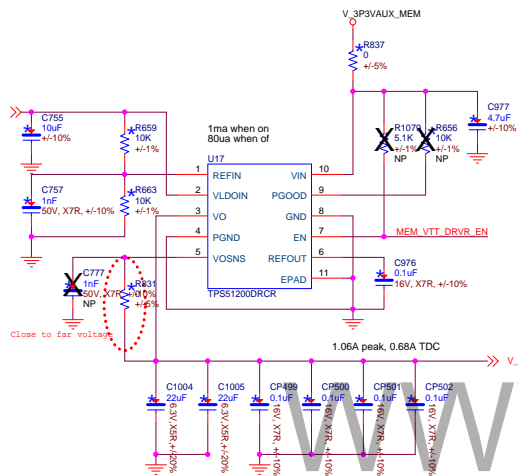
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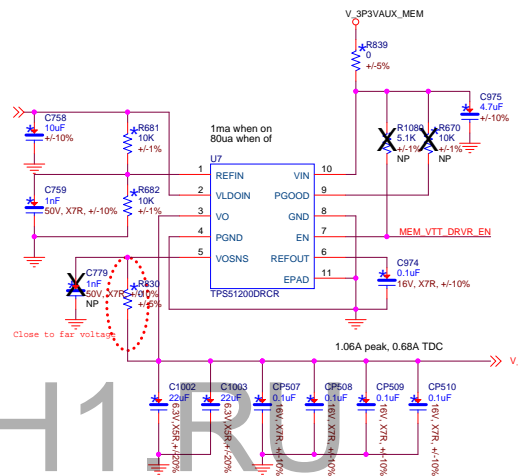
Title
SCHEM, PWA, Bells 3

PN27H

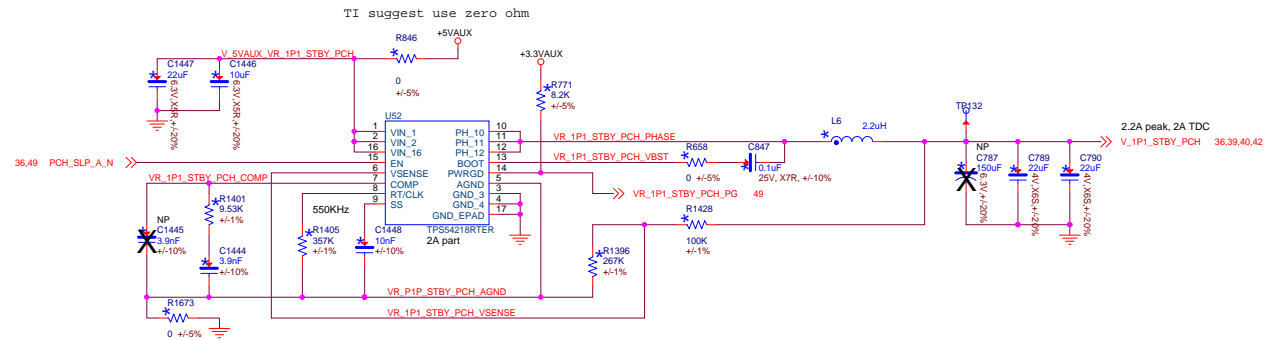
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Note: VCC can be driven from V_5VAUX_MEM if it routs better. -jrs

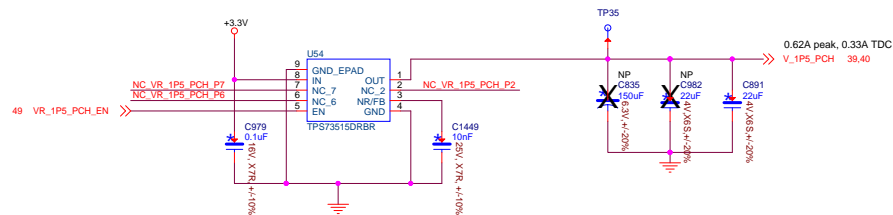


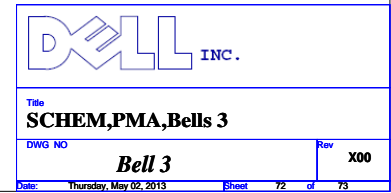
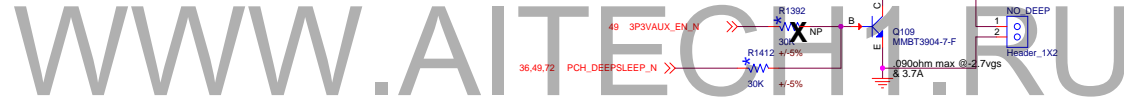
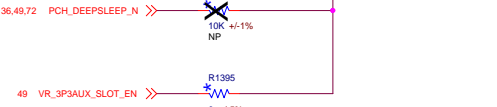
Output	V_1P1_STBY_PCH
Destination	PCH
Input	+5VAUX
Output	1.1V
Max Current	2.0A
Max Current	2.4A
Min Load	
Min OCP	2.9A



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Output	V_1P5_PCH
Destination	PCH
Input	3.3v
Peak Current	620mA
TDP Current	330mA
OCP	800mA
Enabled	



[illegible]

1. 改變部份SATA 連接
2. 增加GPIO26
3. 增加GPIO48
4. dummyR119
5. 更改部份元件reference (power 部份未進行修改)
6. 更新CPU footprint (cpu_lga2011h72 to cpu_lga2011_2h72) 2012/07/23
7. 更新線路頁碼.
8. 修改HDD 連線 (SATA_PCH_4_NB_C_DN to SATA_PCH_4_NB_C_DP)
9. Add and Dummy CP377 and CP378 (Lan modify) 2012/07/26
10. Add RP374, RP375, RP376, RP377 (Lan modify) 2012/07/26
11. add L69/L70 delete RN24/RN25 2012/07/26
12. Add U2.U14.U91.U99.U112.U111.U8.U11.U107.U106.U103.U102.U16 2012/07/26
13. 給部份物料標注添加Module欄. 2012/07/27~30 14. Remove item 10 (Lan) 2012/07/31
15. modify UP19,UP22,UP23 schematic (Lan) 2012/07/31
16. Swap USB3_P0_HS_DN&USB3_P0_HS_DP on RN29
Swap USB3_p0_HS_DN_CONN&USB3_P0_HS_DP_CONN on RN29. (for layout) 2012/08/02
17. Change Mouting Hole Foot Print from
mh40x80_8_dell_giig to mh40x80_8_dell_givvig 2012/08/01
18. 更換FP USB conn 改成與Negril 一致. 2012/08/02
19. change refernece SATA2-ODD4/5
"SATA2-ODD4==> SATA2-ODD0,
"SATA2-ODD5==> SATA2-ODD1" 2012/08/03
20. 修改SATA 3.0 ports footprint sata7_sata3h84 to sata7_sata3h84_p4
21. U_IOEXP,U_EC的footprint修改為dqfn133ch9_v25
22. 修改EC symbol) (Add GND)
23. 修改IOEXP symbol (Add GND)
24. 按照Audio 供應商要求修改線路。
25. reserve xdp &debug display線路
26. 修改CN2 footprint.
27. USB 3.0 HC footprint 修改為qfn69b_1h9
28. Change C1442&C1443 to 22uf
29. Add NPI part.
30. Dummy CATERR_LED,AUX_POWER LED,HD_LED
31. delete U8.
32. Swap USB 3.0 HC signals.
33. 需要在xdp處加一個1.5kohm pull high 電阻 R759
34. Reserve R70
35. 增加UEFI測試點

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